ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ

VISVESVARAYA TECHNOLOGICAL UNIVERSITY

State University of Government of Karnataka Established as per the VTU Act, 1998

"Jnanasangama" Belagavi-590018, Karnataka, India

Prof. Dr. B. E. Rangaswamy, M.A.
REGISTRAR

Phone: (0831) 2498100
Fax : (0831) 2405467

REF: VTU/BGM/ACA/2023-24/ 3252

DATE: 30 SEP 2023

NOTIFICATION

Subject: Tentative Academic Calendar of 1st semester of B.Sc(Hons) program, 3rd and 5th semesters B.E./B.Tech. programs, 4th semester of MBA(IEV) program regarding...

Reference: Hon'ble Vice-Chancellor's approval dated: 30.09.2023

The tentative academic calendar concerned to 1st semester of B.Sc.(Hons) program, 3rd and 5th semesters B.E./B.Tech. programs, 4th semester of MBA(IEV) program for academic year 2023-24 are hereby notified as mentioned below:

	III semester B.E./B.Tech. (2022 scheme)	V semester B.E./ B.Tech. (2021 scheme)	I sem B.Sc(Hons)	IV semester MBA(IEV)*
Commencement of the Semester	25.10.2023	25.10.2023	03.10.2023	09.10.2023
Internship	—	25.10.2023 To 23.11.2023	—	—
Commencement of Classes	25.10.2023	25.11.2023	03.10.2023	09.10.2023
Last Working day of the Semester	10.02.2024	09.03.2024	25.01.2024	27.01.2024
Practical Examination/ Internship Viva Voce/ Project viva	12.02.2024 To 22.02.2024	11.03.2024 To 20.03.2024	29.01.2024 To 09.02.2024	01.02.2024 To 08.02.2024
Theory Examinations	26.02.2024 To 15.03.2024	22.03.2024 To 20.04.2024	12.02.2024 To 01.03.2024	
Commencement of NEXT Semester	18.03.2024	22.04.2024	04.03.2024	——

*Students have to complete skill certification and Internship within this duration (09.10.2023 to 27.01.2024)

Please Note:

- The academic sessions for semesters should commence on the **date mentioned** above.
- If required, the college can plan to have extra classes on 1st and 3rd Saturday and Sundays to complete academic activities within the academic duration mentioned.
- The faculty/staff shall be available to undertake any work assigned by the university.
- Notification regarding the Calendar of Events relating to the conduct of University **Examinations** will be issued by the Registrar (Evaluation) from time to time.
- Academic Calendar **may be modified** based on guidelines/directions issued in the future by UGC/AICTE/State Government.
- Academic Calendar is also applicable for **Autonomous Colleges.** If any changes are to be effected by Autonomous Colleges in the academic terms and examination schedule, they could do so with the approval of the University.
- If any suggestions/clarification/correction, please email to **[illegible]@yahoo.com**

The Principals of Affiliated, Constituent and Autonomous Engineering Colleges, Chairpersons of the University departments are hereby informed to bring the academic calendar to the notice of all concerned.

Sd/-
REGISTRAR

To,

1. The Principals of all affiliated/ constituent /Autonomous Engineering Colleges under the ambit of VTU Belagavi.
2. The chairperson, of the Department of Mechanical Engineering /Civil Engineering /Computer Science and Engineering& Communication Electronics Engineering of the University.

Copy to

1. To the Hon'ble Vice-Chancellor through the secretary to VC, VTU Belagavi for information
2. The Registrar (Evaluation), VTU Belagavi for information.
3. The Regional Directors (I/c) of all the regional offices of VTU for circulation.
4. The Director ITI SMU, VTU Belagavi for information and to make arrangements to upload Academic Calendar on the VTU web portal.
5. The Director of Physical Education, VTU Belagavi for information.
6. The Director, Central Placement Cell, VTU Belagavi for information.
7. The Special Officer Library, VTU Belagavi for information
8. All the concerned Special Officer/s and Caseworker/s of the academic section, VTU, Belagavi

REGISTRAR

ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
VISVESVARAYA TECHNOLOGICAL UNIVERSITY
Phone: 0831 2498100/2405445
Fax: 0831 2405467
Email: registrar@vtu.ac.in
Web: https://vtu.ac.in

No. VTU/BGE/AC PG AP ನಂಅ 82/2023-24/ 2319 Dated: 15 APR 2024

NOTIFICATION

Subject: Tentative Academic Calendar of - IV semester MCA/M.Tech/M/Arch/M.Plan and VI semester B.E./B.Tech. programs academic calendar regarding...

Reference: 01. Dean faculty of Engineering approval dated 16.04.2024
02. The Hon'ble Vice-Chancellor's approval date: 15.04.2024

The tentative Academic Calendar of - IV semester MCA/M.Tech/M/Arch/M.Plan and VI semester B.E./B.Tech., programs are published as below:

	IV semester MCA	IV semester M.Tech.	IV Semester M.Arch.	IV Semester M.Plan.	VI semester B.E./ B.Tech.
Commencement of the Semester	22.04.2024	22.04.2024	22.04.2024	22.04.2024	29.04.2024
Commencement of Classes	22.04.2024	22.04.2024	22.04.2024	22.04.2024	29.04.2024
List Working day of the Semester	27.07.2024	27.07.2024	27.07.2024	27.07.2024	31.07.2024
Practical / Viva-Examination/Internship Viva Voce	28.07.2024 To 29.07.2024				01.08.2024 To 10.08.2024
Theory Examinations	01.08.2024 To 23.08.2024	01.08.2024 To 23.08.2024	29.07.2024 To 03.08.2024	01.08.2024 To 23.08.2024	12.08.2024 To 16.09.2024
Project viva	Will be announced after the submission of the Thesis				—
Submission of the report to university	13.07.2024 To 27.07.2024	01.08.2024 To 20.08.2024	01.08.2024 To 10.08.2024	01.08.2024 To 10.08.2024	—
Commencement of NEXT Semester	—	—	—	—	## 23.09.2024

Commencement of the swapped VII/VIII semester. 50% strength of the students may take up an Internship (VIII sem) immediately after 14.09.2024 and the remaining 50% strength of the students may take up VII semester (23.09.2024)

The principals of all the colleges are hereby informed to bring the content of the NOTIFICATION to the notice of all concerned.

Sd/-
REGISTRAR

Please Note:

- If required, the college can plan to have extra classes on 1st and 3rd Saturdays and Sundays to complete academic activities within the academic duration mentioned.
- Notification regarding the Calendar of Events relating to the conduct of University **Examinations** will be issued by the Registrar (Evaluation) from time to time.
- Academic Calendar **may be modified** based on guidelines/directions issued in the future by UGC/AICTE/State Government.
- The faculty/staff shall be available to undertake any work assigned by the university.
- If any suggestions/clarification please email- **registrar@vtu.ac.in**

To,

The Principals of all the Engineering Colleges under the ambit of the university
The Chairpersons/Program coordinators of the University Departments at Kalaburgi, Bengaluru, Mysuru and Belagavi

Copy to

1. To the Hon'ble Vice-Chancellor through the secretary to VC, VTU Belagavi for information
2. The Registrar (Evaluation), VTU Belagavi for information and needful.
3. The Regional Directors (I/C) of all the regional offices of VTU for circulation.
4. The Director ITI (IMU, VTU Belagavi for information and to make arrangements to upload the Academic Calendar on the VTU web portal.
5. The Director of Physical Education, VTU Belagavi for information
6. The Director, Central Placement Cell, VTU Belagavi for information
7. The Special Officer Library, VTU Belagavi for information
8. All the concerned Special Officer/s and Caseworker/s of the academic section, VTU, Belagavi.
9. Office copy

REGISTRAR

Tentative Revised-Academic Calendar for III and IV Semesters of B.E./B.Tech., programs for the year 2023-24

	Regular Admitted Students	Lateral Entry (Diploma Graduates) Students	Working Professional (Diploma Graduates)	Remarks (Only applicable for students admitted under working professional Category)
Commencement of the 3rd Semester	15.11.2023		12.02.2024	
Commencement of Classes	15.11.2023		12.02.2024	
Last Working day of the 3rd Semester	09.03.2024		13.04.2024	Students have to complete Theory OE only and Practical OE and MC examination.
Practical Examination (Regular Students)	30.03.2024 To 12.04.2024			
Theory Examinations	13.03.2024 To 27.03.2024			
Commencement of 4th Semester	15.04.2024		15.04.2024	
Commencement of the 4th Semester and class	15.04.2024			Students have to complete Theory MC within 15 days at the beginning of the 4th semester
Last Working day of the Semester	27.07.2024			
Practical Examination (Regular Students)	29.07.2024 to 07.08.2024			Common to all
Theory Examinations	08.08.2024 to 28.08.2024			Common to all
Practical Examinations (For Lateral Entry Students)	-----			
Commencement of 5th Semester	02.09.2024			

Please Note:

- If required, the college can plan to have extra classes on 1st and 3rd Saturdays and Sundays to complete academic activities within the academic duration mentioned. For regular and lateral entry, students' academic activities should be conducted as per the academic calendar mentioned above.

MEA Engineering College

Perinthalmanna

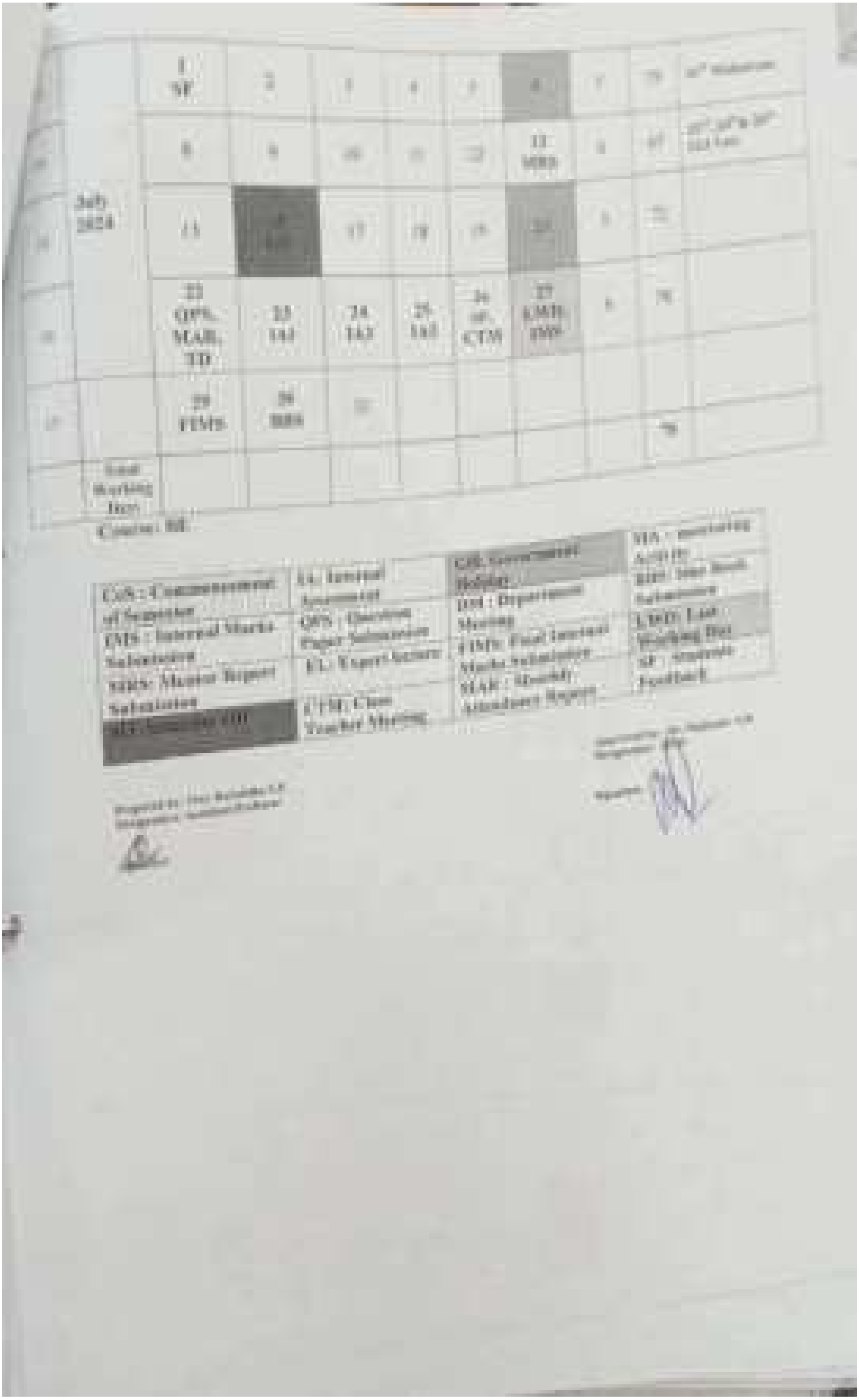
Title: Calendar of Events from [illegible]

[illegible] 2024 – July 2024

Form No.: [illegible]

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Week No.	Semester	Dates						TOTAL NO. OF WORKING DAYS		EVENTS
1	April 2024	22 EOS								
2										
3	May 2024									
4										
5										
6										
7		27 OPN, MAH, ID		29 IA1	30 IA1	31 IA1, CYM				
8	June 2024									
9		3 SB								
10										
11										
12		24 OPN, MAH, ID			27 IA2	28 IA2	29 IA2, CYM			



	M.N. Engineering College Bangalore Title: Calendar of Events [illegible] (April 2024 - July 2024)	Form No. [illegible]

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Week No.	Month	Days						Total No. of Working Days		Events
		MON	TUE	WED	THU	FRI	SAT	Weekly	Cumulative	
1	April 2024		29 COS	30				2	2	
3	May 2024			1 [illegible]	2	3	4	2	[illegible]	1st Labour Day
4		6	7	8	9	10 [illegible]	11 MA	6	[illegible]	10th Basava Jayanthi
5		13	14	15	16	17	18	5	21	
6		20	21	22	23	24	25 MRS	6	27	
7		27	28	29	30	31 CT M		5	32	
8	June 2024						1	0	32	[illegible] IA1 Test
9		3	4 QPS, MAR, TD	5	6 IA1	7 IA1	8 IA1, MA	6	38	
10		10 SF	11	12	13	14	15	5	43	
11		17	18	19	20	21	22 MRS	6	49	
12		24	25	26	27	28	29 CTM	6	54	
13	July 2024	1 QPS, MAR, TD	2	3 IA2	4 IA2	5 IA2	6	5	59	17th Muharram

14		8 SF	9	10	11	12	13 MA	6	65	[illegible]
15		15	16 [illegible]	17	18	19	20	5	70	
16		22	23 QPS, MAR, EL	24	25	26 IA3	27 IA3, MRS	6	76	
17		29 IA3	30 SF, IMS, CTM	31 LWD, FIMS, HBS				5	81	
	Total Working Days								81	

Course: III

CoS: Commencement of Semester	IA: Internal Assessment	GH: Government Holiday	MA – mentoring Activity
IMS: Internal Marks Submission	QPS: Question Paper Submission	DM: Department Meeting	HBS: [illegible] Book Submission
MRS: Mentor Report Submission	EL: Expert lecture	FIMS: Final Internal Marks Submission	LWD: Last Working Day
[illegible]	CTM: Class Teacher Meeting	MAR: Monthly Attendance Report	SF: Students Feedback

Prepared by: Mrs. [illegible]
Designation: Assistant Professor

Approved by: Dr. [illegible]
Designation: HOD

Signature:

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	M.S. Engineering College Bangalore Title: Calendar of Events Odd- III 2023 (Nov 2023 - March 2024)	Form No.: [illegible]

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING (AI-ML)

WEEK NO.	MONTH	DAYS						TOTAL NO. OF WORKING DAYS		EVENTS
		MON	TUE	WED	THU	FRI	SAT	Actual	Cumulative	
1		13 COS	14	15	16	17	[illegible]	6	4	
2	November 2023	20	21	22	23	24	25	6	10	11th & 13th [illegible]
3		27	28	29	[illegible]			4	14	30th Kanakadasa Jayanthi
4						1	[illegible]	1	15	1st CSE Club Activities
5		4	5	6	7	8	9	6	21	25th Christmas
6	December 2023	11	12	13	14	15	[illegible]	5	26	
7		18	19	20	21	22	23	6	32	
8		[illegible]	26	27	28	29	30	5	37	
9		1	2	3	4	5	[illegible]	5	42	15th Makara Sankranti
10	January 2024	8	9 QPS	10	11 IA1	12 IA1	13	6	48	26th Republic Day
11		[illegible]	16	17	18	19	20	4	52	IA1 Test
12		22	23	24	25	[illegible]	27	5	57	

13		29	30	31				3	60	
14					1	2		2	62	8th Expert Talkative on MSME Schemes
15		5	6	7	8	9	10	8	68	
16	February 2024	12	13	14 IAS	15 IAS	16		9	73	IAS Test
17		19	20	21	22	23	24	6	79	
18		25	26	27	28	29				
19						1				IAS Test
20		4 IAS	5 IAS	6	7	8	LWD			
	Total Working Days								85	

Course: BE

CoS : Commencement of Semester	IA: Internal Assessment	GH/Government Holiday	MA – mentoring Activity
IMS : Internal Marks Submission	QPS : Question Paper Submission	DM : Department Meeting	BBS: Idea Book Submission
MRS: Mentor Report Submission	EL: Expert lecture	FIMS: Final Internal Marks submission	LWD: Last Working Day
SEMESTER END	CTM: Class Teacher Meeting	MAR : Monthly Attendance Report	SF : Students Feedback

Prepared by: Mrs. Ravikala S.P.
Designation: Assistant Professor

Signature

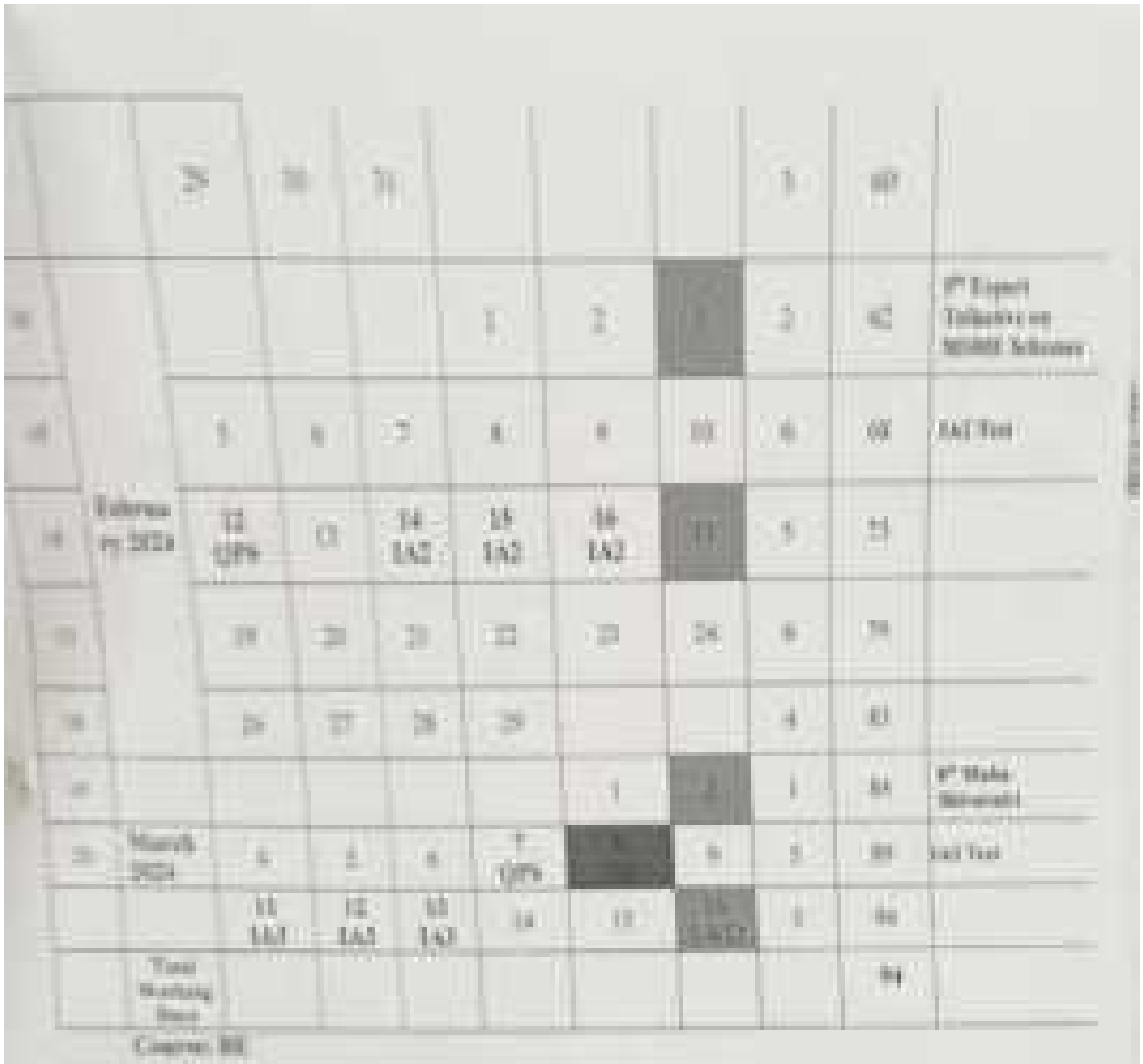
Approved by: Dr. Mahesh S.H
Designation: HOD

Signature

	M.S. Engineering College	Form No:
	Bangalore	R/ TP 03/ 12/ 01
	Title: Calendar of Events Odd -V SEM	
	(Nov 2023 - March 2024)	

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING (AI/ML)

Wk No.	Month	DAYS						TOTAL NO OF WORKING DAYS		EVENTS
		MON	TUE	WED	THU	FRI	SAT	General	Cumulative	
1	November 2023	13 COS	14	15	16	17	18	4	4	
2		20	21	22	23	24	25	6	10	12th & 13th Diwali
3		27	28	29	[illegible]			4	14	30th Kanakadasa Jayanthi
4	December 2023					1	2	1	15	21st CSE Club Activities
5		4	5	6	7	8	9	6	21	25th Christmas
6		11	12	13	14	15	16	5	26	
7		18	19	20	21	22	23	6	32	
8		[illegible]	26	27	28	29	30	5	37	
9	January 2024	1	2	3	4	5	6	5	42	15th Makara Sankaranti
10		8	9	10	11	12 QPS	13	6	48	26th Republic Day
11		[illegible]	16	17 IA1	18 IA1	19 IA1	20	4	52	IA1 Test
12		22	23	24	25	[illegible]	27	5	57	



CoE : Commencement of Semester	IA: Internal Assessment	CIE: Continuous Evaluation	MA – mentoring Activity
DHA : Internal Marks Submission	QPS : Question Paper Submission	DW : Department Meeting	BBS: Blue Book Submission
MRE: Mantra Report Submission	EL: Expert lecture	FIMS: Final Internal Marks Submission	LWD: Last Working Day
SW: Summer Vacation	CTM: Class Teacher Meeting	MAR : Monthly Attendance Report	SF : Students Feedback

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MS Engineering College, Bangalore
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

Course Information File

Semester & Year: III & 2023

Subject Name: **Digital Design and Computer Organization**	*Subject Code*: BCS302
Total Teaching Hours: **40 hrs.**	*Duration of Exam*: 03
Exam Marks: 50	*IA Marks*: 50
Lesson Plan Author: **Mrs. Sneha Jewargi**	
Designation: **Assistant Professor**	
Number of times taught this subject :1	
Verified by:	*Date*: 06/03/2023

Course objectives:

- To demonstrate the functionalities of binary logic system
- To explain the working of combinational and sequential logic system
- To realize the basic structure of computer system
- To illustrate the working of I/O operations and processing unit

Course Outcomes: At the end of the course, the student will be able to:

Sl. No	Course Outcomes	Bloom's Taxonomy Level
CO1	Apply the K-Map techniques to simplify various Boolean expressions.	L1
CO2	Design different types of combinational and sequential circuits along with Verilog programs.	L2
CO3	Describe the fundamentals of machine instructions, addressing modes and Processor performance.	L3
CO4	Explain the approaches involved in achieving communication between processor and I/O devices.	L4
CO5	Analyze Internal Organization of Memory and impact of cache/Pipelining on Processor Performance.	L5

Teaching Pedagogy:

1. Lecture.
2. Assignment.
3. Class Discussion.
4. Course Examination.
5. Tutorial.
6. Quiz.
7. Seminars

Mapping of Graduate Attributes to Course Outcomes (COs):

	Program Outcomes												Program Specific Outcomes	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
Course Outcomes	Engineering knowledge	Problem analysis	Design/development of solution	Conduct investigations of complex problems	Modern tool usage	The engineer and society	Environment and sustainability	Ethics	Individual and team work	Communication	Project management and finance	Life-long learning	Problem Solving Skill	Professional Skill
CO1:	L	M	M										M	
CO2:	M	M	M	M							L	L	M	M
CO3:	M	L	M	L							L	M	M	L
CO4:	M	M	M								L	M	M	M
CO5:	H	L	M	L							L	M	M	M

Degree of Compliance:

High (H) : Greater than 70%
Medium (M) : Between 40 to 69%
Low (L) : Between 00 to 39%

Syllabus Content

Subject Code: BCS302 **IA: 50**

Subject Name: Digital Design and Computer Organization **Exam Marks: 50**

Teaching Hours: 40

Topics	Hours	% of Portion Covered	
		Chapter wise	Cumulative
Module – 1 **Introduction to Digital Design:** Binary Logic, Basic Theorems And Properties Of Boolean Algebra, Boolean Functions, Digital Logic Gates, Introduction, The Map Method, Four-Variable Map, Don't-Care Conditions, NAND and NOR Implementation, Other Hardware Description Language – Verilog Model of a simple circuit	08 hours	20	20
Module – 2 **Combinational Logic:** Introduction, Combinational Circuits, Design Procedure, Binary Adder- Subtractor, Decoders, Encoders, Multiplexers. HDL Models of Combinational Circuits – Adder, Multiplexer, Encoder. **Sequential Logic:** Introduction, Sequential Circuits, Storage Elements: Latches, Flip-Flops.	08 hours	20	40
Module – 3 **Basic Structure of Computers:** Functional Units, Basic Operational Concepts, Bus structure, Performance – Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement. **Machine Instructions and Programs:** Memory Location and Addresses, Memory Operations, Instruction and Instruction sequencing, Addressing Modes.	08 hours	20	60
Module – 4 **Input/output Organization:** Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Direct Memory Access: Bus Arbitration, Speed, size and Cost of memory systems, Cache Memories – Mapping Functions.	08 hours	20	80
Module – 5 **Basic Processing Unit:** Some Fundamental Concepts: Register Transfers, Performing ALU operations, fetching a word from Memory, Storing a word in memory, Execution of a Complete Instruction.	08 hours	20	100

Pipelining: Basic concepts, Role of Cache memory, Pipeline Performance.			

TEXT BOOKS:

1. M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.
2. Carl Hamacher, ZvonkoVranesic, SafwatZaky, Computer Organization, 5 th Edition, Tata McGraw Hill.

Web links and Video Lectures (e-Resources):
https://cse11-iiith.vlabs.ac.in/

EVALUATION SCHEME:

IA SCHEME	
Assessment	**Weightages in Marks**
Internal Assessment Exam 1	25
Internal Assessment Exam 2	25
Improvement- Internal Assessment Exam 3	25
Final Internal Assessment Marks	Average of Two
Assignments/Seminar etc	10
Total (Average + Assignment/Seminar etc)	25
Laboratory Record & conduction of experiment	15
Lab test	10
Total	25
IPCC Total	50

SUBJECT UTILIZATION FOR IA EXAMS:

Module	Chapter	Teaching Hours	No. of Questions in		
			IA Exam I	IA Exam II	IA Exam III
1, 2	Introduction to Digital Design	10	VTU Exam Pattern (Answer any two full questions choosing any one question from each part)		
	Combinational logic and sequential logic	10			
3, 4	Basic structure of computers and Instructions and programs	10			
	Input/Output Organization	10			
5	Basic Processing unit: Pipelining	10			

Module Wise Plan

Subject Name: Digital Design and Computer Organization **Subject Code: BCS302**

Module Name and Title: 1. Introduction to Digital design

Learning Objectives:

At the end of this chapter student should be able to:

1. Explain the basic theorem and properties of Boolean algebra.
2. Design the digital logic gates.
3. Perform the k-map problems.
4. Explain the NAND and NOR gate implementation.
5. Explain the steps in HDL program.

Learning Outcomes:

1. Understanding the digital logic gates
2. Understanding how to solve K-map using different variables.
3. Understanding how to implement NAND and NOR gates.
4. Understanding the steps of HDL programming.

Lesson Schedule:

Class Number	Portion covered	Book	Page No.
1	Introduction to Digital Design: Binary Logic, Basic Theorems And Properties Of Boolean Algebra.	T1	30-50
2	Boolean Functions, Digital Logic Gates.	T1	45-65
3,4	Introduction, The Map Method, Three-Variable K-map	T1	73-79
5,6	Four variable K-map.	T1	80-87
7,8	Don't care conditions.	T1	88-90
9	NAND and NOR Implementation.	T1	90-102
10	Other Hardware Description Language – Verilog Model of a simple circuit.	T1	108-118

	Questions	Blooms Taxonomy
1	With symbol, truth table and Boolean expression explain a) AND gate b) OR gate c) NOT gate d)XOR gate e)NAND GATE	L1
2	Explain basic theorem and properties of Boolean algebra?	L1
3	Realize the function using only two input NAND gate and inverter i) f1=$\sum$m(0,2,3,4,5) ii) f2=$\sum$m(1,2,6,7)	L1
4	F(P, Q,R,S)=$\sum$m(0,3,5,6,7,11,14). Write the SOP and logic diagram.	L2
5	F(A,B,C,D)=$\sum$m(1,2,3,5,6,7,11,12,13,14,15). Draw the logic diagram.	L2
6	F(w,x,y,z)=$\sum$m(7,9,12,13,14,15)+d(4,11)	L2
7	F(ABCD)=$\sum$m(0,1,2,3,10,11,12,13,14,15)	L2
8	Realize the given function F=$\bar{b}\bar{c}$+a$\bar{b}$+$\bar{a}$b	L2

9	F(WXYZ)=$\overline{XZ}$+WYZ+$\overline{WYZ}$+$\overline{XY}$. Realize the given function	L2
10	Y = ABCD+ $\overline{ABCD}$ + A$\overline{BC}$ + $\overline{AB}$	L2

Module Name and Title: 2. Combinational and Sequential circuit

Learning Objectives:

At the end of this chapter student should be able to:

1. Explain the combinational circuit.
2. Explain how to design Adder and Subtractor.
3. Explain the decoder, encoder and multiplexer.
4. Explain the steps to write HDL program code.
5. Explain the Methods of sequential circuit.
6. Explain the implementation of latches and flip-flops.

Learning Outcomes:

1. Understanding the combinational circuit.
2. Understanding how to implement Adder, Subtracter.
3. Understanding how to design Decoder, Encoder and Multiplexer.
4. Understanding the steps to write HDL programs.
5. Understanding the design method of sequential circuit.
6. Understanding the design concept and implementation of latches and flip-flops.

Lesson Schedule:

Class Number	Portion covered	Book	Page No.
11	**Introduction: Combinational Circuits**	T1	125-127
12	Design Procedure: Binary Adder	T1	129-141
13	Subtractor, Decoders	T1	141-154
14	Encoders, Multiplexers	T1	155-163
15	HDL Models of Combinational Circuits – Adder, Multiplexer, Encoder.	T1	164-181
16	Sequential Logic: Introduction, Sequential Circuits.	T1	190-192
17	Storage Elements: Latches	T1	193-196
18	Flip-Flops.	T1	196-203

	Questions	Blooms Taxonomy
1	Design a Full adder by constructing truth table, logic diagram and simplify the output equation.	L2
2	Design and explain half subtractor.	L2
3	Explain the working principle of 4 bit binary adder with carry propagation.	L2
4	Explain multiplexer with the help of logic diagram and corresponding expression.	L2
5	Briefly explain with neat diagram 3:8 decoder.	L2
6	Explain in brief history of HDL and structure of HDL module.	L1
7	Explain the full subtractor with circuit diagram and expression.	L2
8	What is VHDL? show how to model 4:1 MUX using VHDL conditional assignment statement.	L2
9	Using structural model, write VHDL code for Half adder	L2
10	Explain structure of VHDL program. Write VHDL code for 4-bit parallel adder using full adder as component.	L2
11	Explain working of SR latch using NOR gates.	L3
12	Explain with neat diagram, working of JK flip flop and derive the characteristics equation.	L3
13	Derive characteristics equation for the following flip flops i) SR flip flop ii) D flip flop iii) T flip flop iv) JK flip flop	L3

Module Name and Title: 3. Basic structure of computers

Learning Objectives:

At the end of this chapter student should be able to:

1. Explain the meaning and types of functional units of computer.
2. Explain the Stages of bus structure.
3. Explain the Role of performance of clock in processor.
4. Explain the machine instructions and program.
5. Explain different types of addressing modes.

Learning Outcomes:

1. Understanding the meaning and operational concepts.

2. Understanding the Performance of processor clock.
3. Understanding the machine instruction and program.
4. Understanding the instruction and addressing modes.

Lesson Schedule:

Class Number	Portion covered	Book	Page No.
19	Functional Units, Basic Operational Concepts.	T2	2-7
20	Bus structure, Performance – Processor Clock	T2	9-14
21	Basic Performance Equation, Clock Rate.	T2	14-16
22	Performance Measurement, Machine Instructions and Programs.	T2	17-20
23	Memory Location and Addresses.	T2	33-36
24	Memory Operations, Instruction and Instruction sequencing.	T2	36-44
25	Addressing Modes.	T2	48-56

	Questions	Blooms Taxonomy
1	With a neat diagram describe the functional unit of computer.	L1, L2
2	Explain the basic operational concept between processor and memory with neat diagram.	L2
3	Explain various parameters that affects the performance of a computer and also provide the basic performance equation.	L2
4	Explain bus structure.	L2
5	Write a note on processor clock.	L2
6	Explain how to measure the performance of computer.	L2
7	Explain the i) one address instruction ii)two address instruction iii)three address instruction with example?	L2
8	Define byte addressability, Big-Endian and Little-Endian assignment briefly.	L2
9	Explain memory location addressing.	L2
10	Explain memory operation with example.	L2
11	Illustrate instruction and instruction sequential with example.	L2
12	Explain conditional codes with example.	L2
13	Discuss the following addressing modes with example i) Immediate ii) Register iii)Direct iv)Indirect v)Index	L2

Module Name and Title: 4. Input/output Organization

Learning Objectives:

At the end of this chapter student should be able to:

1. Explain the memory mapping and I/O mapping.
2. Explain the need of Interrupt.
3. Explain the Direct Memory Access.
4. Explain the concept of Bus Arbitration.
5. Explain the cache memory and memory mapping.

Learning Outcomes:

1. Understanding the memory mapping and I/O mapping.
2. Understanding the significance of Interrupt.
3. Understanding the concept of Direct memory Access.
4. Understanding the importance of Bus Arbitration.
5. Understanding the concept of cache memory and memory mapping.

Lesson Schedule:

Class Number	Portion covered	Book	Page No.
26	Accessing I/O Devices	T2	204-205
27	Interrupts – Interrupt Hardware	T2	205-210
28,29	Enabling and Disabling Interrupts, Handling Multiple Devices.	T2	211-213
30	Direct Memory Access	T2	234-236
31	Bus Arbitration	T2	237-240
32	Speed, size and Cost of memory systems.	T2	313
33	Cache Memories	T2	313-315
34	Mapping Functions	T2	316-321

	Questions	Blooms Taxonomy
1	Write a note on single bus structure with neat diagram.	L2
2	Explain the concept of memory map I/O and I/O interface with neat diagram.	L1

3	Write a note on i) Interrupt hardware ii) Interrupt nesting.	L2
4	Explain the following i)vectre interrupt ii) simultaneous request .	L2
5	Define Interrupt. Point out and explain the various types of enabling and disabling interrupt.	L2
6	Explain the following method of handling interrupt from multiple devices. (i) Diasy chain (ii) Priority structure.	L2
7	Explain operation of DMA with neat diagram.	L2
8	Define Bus arbitration? Explain centralized arbitration mechanism in DMA with a neat diagram.	L2
9	Explain the distributed arbitration mechanism in DMA with a neat diagram.	L2
10	Define cache memory? Explain various types with neat diagram.	L2
11	What is mapping? Explain set associative technique with neat diagram.	L2
12	What is cache memory? Explain direct mapping.	L2

Module Name and Title: **5. Basic Processing Unit**

Learning Objectives:

At the end of this chapter student should be able to answer:

1. Explain the fundamental concept of processing unit.
2. Explain the steps in performing ALU operation.
3. Explain how to fetch and store a word in memory.
4. Explain the basic concept of pipelining.
5. Explain the role of cache memory.
6. Explain the pipeline performance.

Learning Outcomes:

1. Understanding the fundamental concepts of processing unit.
2. Understanding the steps in performing ALU operation and register transfer.
3. Understanding how to fetch, store and execution of a word in memory.
4. Understanding the basic concept of pipelining.
5. Understanding the role of cache memory.
6. Understanding the pipelining performance.

M S ENGINEERING COLLEGE, BENGALURU

Title: Time Table

Form No: [illegible]

Effective date: [illegible]

Department: COMPUTER SCIENCE AND ENGINEERING

Room No: [illegible]

Semester: IV SEM A Sec | CLASS TEACHER: Mrs. Sneha Jewargi

	9:00am to 9:55am	9:55am to 10:50am		11:05am to 12:00pm	12:00pm to 12:55pm		1:45pm to 2:40pm	2:40pm to 3:35pm	3:35pm to 4:30pm
	1	2		3	4		5	6	7
MONDAY	ADA(B1-LAB 018)/DBMS(B2-LAB 114)/MP(B3-LAB 118)		TEA BREAK (10:50 AM TO 11:05 AM)	DMS	BIOLOGY	LUNCH BREAK (12:55 PM TO 1:45 PM)	ADA	NSS/PE/Yoga	NSS/PE/Yoga
TUESDAY	ADA	MP		DBMS (B1-LAB 114)/ MP(B2-LAB 118)/LATEX(B3-LAB 013)			DMS	PMKY TRAINING	PLACEMENT AND TRAINING
WEDNESDAY	MP	DBMS		ADA	DMS		MP (B1-LAB 118)/LATEX (B2-LAB 013)/ADA(B3-LAB 018)		PLACEMENT AND TRAINING
THURSDAY	DBMS	ADA		DMS	DBMS		ADA (B3-LAB 018)/ DBMS (B1-LAB 114)/ LATEX (B2-LAB 013)		PMKY TRAINING
FRIDAY	UHV	DBMS		MP	MP		BIOLOGY	PMKY TRAINING	PLACEMENT AND TRAINING
SATURDAY	ADA	MP		DBMS	DMS		TUTORIAL	TUTORIAL	TUTORIAL

SL.NO.	SUBJECT NAME	SUBJECT CODE	FACULTY NAME	TOTAL NUMBER OF HOURS L	T	P
1	Analysis & Design of Algorithms	BCS401	Mr Narayan H M	4	1	-
2	Microcontrollers	BCS402	Mrs. Sneha Jewargi	4	1	2
3	Database Management Systems	BCS403	Mrs. Prabha S Naik	4	1	2
			Mrs. Harshitha S P(LAB)	-	-	2
4	Analysis & Design of Algorithms Lab	BCSL404	Mr Narayan H M	2	1	-
5	Discrete Mathematical Structures	BCS405A	Mrs. Bhagya M	-	-	2
6	Technical writing using LATEX	BCS456D	Ms. Aishwarya M	2	-	-
7	Biology For Engineers	BBOK407	Mrs. Shwetha K S	1	-	-
9	Universal Human Values	BUHK408	Mr. Rajeesh	0	0	2
10	National Service Scheme (NSS)/ Physical Education (PE) (Sports and Athletics)/ Yoga	BNSK459/ BPEK459/ BYOK459	Mr. Rajesh			

PREPARED BY: PRABHA S. NAIK	VERIFIED BY: Dr. MALATESH S. H.	APPROVED BY: Dr. P. MAHADEVASWAMY
DESIGNATION: ASSOCIATE PROFESSOR	DESIGNATION: HOD	DESIGNATION: PRINCIPAL
SIGNATURE:	SIGNATURE:	SIGNATURE:

	M S ENGINEERING COLLEGE, BENGALURU	Form No:
	Title: Time Table	

Department: COMPUTER SCIENCE AND ENGINEERING		Effective Date: 29/01/2024
Semester: VI	CLASS TEACHER: Mrs. Dipti Patnayak	Room No:107

	9:00am to 9:55am	9:55am to 10:50am	TEA BREAK 10:50 AM TO 11:05 AM	11:05am to 12:00pm	12:00pm to 12:55pm	LUNCH BREAK 01:55 PM TO 2:50 PM	2:50pm to 3:45pm	3:45pm to 4:40pm	4:40pm to 5:35pm
	1	2		3	4		5	6	7
MONDAY	CNR	AT		CG(A3-LAB 114)/Mini Project(A2)			FS	FS (A3-LAB 017)	
TUESDAY	AT	CG & IP		AT	SE & PM		PLACEMENT AND TRAINING	PLACEMENT AND TRAINING	PMKY TRAINING
WEDNESDAY	CNR	SE & PM		FS	CG & IP		FS (A2-LAB 017)/ CG(A3-LAB 114)/ Mini Project (A3)		PLACEMENT AND TRAINING
THURSDAY	CG & IP	FS		CNR	SE & PM		AT	INTERNSHIP	INTERNSHIP
FRIDAY	CNR	SE & PM		FS(A3-LAB 017)/CG(A2-LAB 114)/Mini Project(A3)			FS	CG & IP	PMKY TRAINING
SATURDAY	CG & IP	DS & A		SE & PM	CNR		TUTORIAL	TUTORIAL	TUTORIAL

SL.NO.	SUBJECT NAME	SUBJECT CODE	FACULTY NAME	TOTAL NUMBER OF HOURS		
				L	T	P
1	Software Engineering & Project Management	21CS61	Dr Mahesh K H	4	1	-
2	Full Stack Development	21CS62	Mrs. Harshitha S P	4	1	2
3	Computer Graphics and Fundamentals of Image Processing	21CS63	Dr. Rajan P	4	1	-
4	Agile Technology	21CS641	Mrs. Dipti Patnayak	4	1	-
5	Conservation of Natural Resources	21CV654	Mr. Murali Krishna	4	1	-
6	Computer Graphics and Fundamentals of Image Processing Laboratory	21CSL66	Dr. Rajan P	-	-	2
7	Mini Project	21CS69P67	Mrs. Dipti Patnayak	-	-	2
8	Innovation Entrepreneurship /Societal Internship	21INT68	Mrs. Dipti Patnayak	-	-	2

PREPARED BY: PRABHA S NAIK	VERIFIED BY: Dr. MALATESH S H	APPROVED BY: Dr. P. MAHADEVASWAMY
DESIGNATION: ASSOCIATE PROFESSOR	DESIGNATION: HOD	DESIGNATION: PRINCIPAL
SIGNATURE:	SIGNATURE:	SIGNATURE:

Principal
M.S. Engineering College
Navarathna Agrahara, Sadashiva Post,
Bangalore-560 110

[illegible] COLLEGE BENGALURU

Time Table

Form No. [illegible]

Department : COMPUTER SCIENCE & ENGINEERING

Semester: VIII SEM CSE [illegible]

CLASS TEACHER: Ms. Aishwarya M

Effective Date : [illegible]

Room No : LE [illegible]

	9:00 AM TO 9:55 AM	9:55 AM TO 10:50 AM		11:05 AM TO 12:00 PM	12:00 PM TO 12:55 PM		1:40 PM TO 2:40 PM	2:40 PM TO 3:40 PM	3:40 PM TO 4:30 PM
	1	2	10:50AM TO 11:05AM TEA BREAK	3	4	12:55 PM TO 1:40 PM LUNCH BREAK	5	6	7
MONDAY	-	SAN		IoT	IoT		Internship		
TUESDAY	-	IoT		SAN	SAN		Technical Seminar		
WEDNESDAY	Project Work Phase - 2			Project Work Phase - 2			Project Work Phase - 2		
THURSDAY	Technical Seminar			Technical Seminar			Technical Seminar		
FRIDAY	Project Work Phase - 2			Project Work Phase - 2			Project Work Phase - 2		
SATURDAY	Project Work Phase - 2 /Technical Seminar / Internship			Project Work Phase - 2 /Technical Seminar / Internship			Internship		

Sl. No.	SUBJECT NAME	SUBJECT CODE	FACULTY NAME	L	T	P
1	Internet of Things	18CS81	Ms. Aishwarya M	3	-	-
2	Storage Area Networks	18CS822	Dr. Malatesh S.H	3	-	
3	Project Work Phase - 2	18CSP83	Dr. Malatesh S.H	-	-	2
4	Technical Seminar	18CSS84	Dr. Malatesh S.H	-	-	2
5	Internship	18CSI85	[illegible]	-	-	-

PREPARED BY: Mrs. PRABHA NAIK	VERIFIED BY: Dr. MALATESH S.H.	APPROVED BY: Dr. P. MAHABOOVANADEVI [illegible]
DESIGNATION: ASSOCIATE PROFESSOR	DESIGNATION: HOD	DESIGNATION: PRINCIPAL
SIGNATURE:	SIGNATURE:	SIGNATURE:

MS Engineering College, Bangalore
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

Course Information File

Semester & Year: III & 2023

Subject Name: **Digital Design and Computer Organization**	*Subject Code*: BCS302
Total Teaching Hours: **40 hrs.**	*Duration of Exam*: 03
Exam Marks: 50	*IA Marks*: 50
Lesson Plan Author: **Mrs. Sneha Jewargi**	
Designation: **Assistant Professor**	
Number of times taught this subject :1	
Verified by:	*Date*: 06/03/2023

Course objectives:

- To demonstrate the functionalities of binary logic system
- To explain the working of combinational and sequential logic system
- To realize the basic structure of computer system
- To illustrate the working of I/O operations and processing unit

Course Outcomes: At the end of the course, the student will be able to:

Sl. No	Course Outcomes	Bloom's Taxonomy Level
CO1	Apply the K-Map techniques to simplify various Boolean expressions.	L1
CO2	Design different types of combinational and sequential circuits along with Verilog programs.	L2
CO3	Describe the fundamentals of machine instructions, addressing modes and Processor performance.	L3
CO4	Explain the approaches involved in achieving communication between processor and I/O devices.	L4
CO5	Analyze Internal Organization of Memory and Impact of cache/Pipelining on Processor Performance.	L5

Teaching Pedagogy:

1. Lecture.
2. Assignment.
3. Class Discussion.
4. Course Examination.
5. Tutorial.
6. Quiz.
7. Seminars

Mapping of Graduate Attributes to Course Outcomes (COs):

	Program's Outcomes												Program Specific Outcomes	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
Course Outcomes	Engineering knowledge	Problem analysis	Design/development of solutions	Conduct investigations of complex problems	Modern tool usage	The engineer and society	Environment and sustainability	Ethics	Individual and team work	Communication	Project management and finance	Life-long learning	Problem Solving Skill	Professional Skill
CO1:	L	M	M										M	
CO2:	M	M	M	M							L	L	M	M
CO3:	M	L	M	L							L	M	M	L
CO4:	M	M	M								L	M	M	M
CO5:	H	L	M	L							L	M	M	M

Degree of Compliance:

High (H) : Greater than 70%
Medium (M) : Between 40 to 69%
Low (L) : Between 00 to 39%

Syllabus Content

Subject Code: BCS302 **IA: 50**

Subject Name: Digital Design and Computer Organization **Exam Marks: 50**

Teaching Hours: 40

Topics	Hours	% of Portion Covered	
		Chapter wise	Cumulative
Module – 1 **Introduction to Digital Design:** Binary Logic, Basic Theorems And Properties Of Boolean Algebra, Boolean Functions, Digital Logic Gates, Introduction, The Map Method, Four-Variable Map, Don't-Care Conditions, NAND and NOR Implementation, Other Hardware Description Language – Verilog Model of a simple circuit	08 hours	20	20
Module – 2 **Combinational Logic:** Introduction, Combinational Circuits, Design Procedure, Binary Adder- Subtractor, Decoders, Encoders, Multiplexers. HDL Models of Combinational Circuits – Adder, Multiplexer, Encoder. **Sequential Logic:** Introduction, Sequential Circuits, Storage Elements: Latches, Flip-Flops.	08 hours	20	40
Module – 3 **Basic Structure of Computers:** Functional Units, Basic Operational Concepts, Bus structure, Performance – Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement. **Machine Instructions and Programs:** Memory Location and Addresses, Memory Operations, Instruction and Instruction sequencing, Addressing Modes.	08 hours	20	60
Module – 4 **Input/output Organization:** Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Direct Memory Access: Bus Arbitration, Speed, size and Cost of memory systems, Cache Memories – Mapping Functions.	08 hours	20	80
Module – 5 **Basic Processing Unit:** Some Fundamental Concepts: Register Transfers, Performing ALU operations, fetching a word from Memory, Storing a word in memory. Execution of a Complete Instruction.	08 hours	20	100

Pipelining: Basic concepts, Role of Cache memory, Pipeline Performance.			

TEXT BOOKS:

1. M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.
2. Carl Hamacher, ZvonkoVranesic, SafwatZaky, Computer Organization, 5 th Edition, Tata McGraw Hill.

Web links and Video Lectures (e-Resources):
https://vtu11-6th.vlabs.ac.in/

EVALUATION SCHEME:

IA SCHEME	
Assessment	**Weightages in Marks**
Internal Assessment Exam 1	25
Internal Assessment Exam 2	25
Improvement- Internal Assessment Exam 3	25
Final Internal Assessment Marks	Average of Two
Assignments/Seminar etc	10
Total (Average + Assignment/Seminar etc)	25
Laboratory Record & conduction of experiment	15
Lab test	10
Total	25
IPCC Total	50

SUBJECT UTILIZATION FOR IA EXAMS:

Module	Chapter	Teaching Hours	No. of Questions in		
			IA Exam I	IA Exam II	IA Exam III
1, 2	Introduction to Digital Design	10	VTU Exam Pattern (Answer any two full questions choosing any one question from each part)		
	Combinational logic and sequential logic	10			
3, 4	Basic structure of computers and Instructions and programs	10			
	Input/Output Organization	10			
5	Basic Processing unit, Pipelining	10			

Module Wise Plan

Subject Name: Digital Design and Computer Organization **Subject Code: BCS302**

Module Name and Title: 1. Introduction to Digital design

Learning Objectives:

At the end of this chapter student should be able to:

1. Explain the basic theorem and properties of Boolean algebra.
2. Design the digital logic gates.
3. Perform the k-map problems.
4. Explain the NAND and NOR gate implementation.
5. Explain the steps in HDL program.

Learning Outcomes:

1. Understanding the digital logic gates
2. Understanding how to solve K-map using different variables.
3. Understanding how to implement NAND and NOR gates.
4. Understanding the steps of HDL programming.

Lesson Schedule:

Class Number	Portion covered	Book	Page No.
1	Introduction to Digital Design: Binary Logic, Basic Theorems And Properties Of Boolean Algebra.	T1	30-50
2	Boolean Functions, Digital Logic Gates.	T1	45-65
3,4	Introduction, The Map Method, Three-Variable K-map	T1	73-79
5,6	Four variable K-map.	T1	80-87
7,8	Don't care conditions.	T1	88-90
9	NAND and NOR Implementation.	T1	90-102
10	Other Hardware Description Language – Verilog Model of a simple circuit.	T1	108-118

	Questions	Blooms Taxonomy
1	With symbol, truth table and Boolean expression explain a) AND gate b) OR gate c) NOT gate d)XOR gate e)NAND GATE	L1
2	Explain basic theorem and properties of Boolean algebra?	L1
3	Realize the function using only two input NAND gate and inverter i) $f1=\sum m(0,2,3,4,5)$ ii) $f2=\sum m(1,2,6,7)$	L1
4	$F(P, Q,R,S)=\sum m(0,3,5,6,7,11,14)$. Write the SOP and logic diagram.	L2
5	$F(A,B,C,D)=\sum m(1,2,3,5,6,7,11,12,13,14,15)$. Draw the logic diagram.	L2
6	$F(w,x,y,z)=\sum m(7,9,12,13,14,15)+d(4,11)$	L2
7	$F(ABCD)=\sum m(0,1,2,3,10,11,12,13,14,15)$	L2
8	Realize the given function $F=\bar{b}\bar{c}+a\bar{b}+\bar{a}b$	L2

9	F(WXYZ)=$\overline{XZ}$+WYZ+$\overline{WYZ}$+$\overline{XY}$. Realize the given function	L2
10	Y = ABCD+ $\overline{ABCD}$ + A$\overline{BC}$ + $\overline{AB}$	L2

Module Name and Title: 2. Combinational and Sequential circuit

Learning Objectives:

At the end of this chapter student should be able to:

1. Explain the combinational circuit.
2. Explain how to design Adder and Subtractor.
3. Explain the decoder, encoder and multiplexer.
4. Explain the steps to write HDL program code.
5. Explain the Methods of sequential circuit.
6. Explain the implementation of latches and flip-flops.

Learning Outcomes:

1. Understanding the combinational circuit.
2. Understanding how to implement Adder, Subtractor.
3. Understanding how to design Decoder, Encoder and Multiplexer.
4. Understanding the steps to write HDL programs.
5. Understanding the design method of sequential circuit.
6. Understanding the design concept and implementation of latches and flip-flops.

Lesson Schedule:

Class Number	Portion covered	Book	Page No.
11	**Introduction: Combinational Circuits**	T1	125-127
12	Design Procedure: Binary Adder	T1	129-141
13	Subtractor, Decoders	T1	141-154
14	Encoders, Multiplexers	T1	155-163
15	HDL Models of Combinational Circuits – Adder, Multiplexer, Encoder.	T1	164-181
16	Sequential Logic: Introduction, Sequential Circuits.	T1	190-192
17	Storage Elements: Latches	T1	193-196
18	Flip-Flops.	T1	196-203

	Questions	Blooms Taxonomy
1	Design a Full adder by constructing truth table, logic diagram and simplify the output equation.	L2
2	Design and explain half subtractor.	L2
3	Explain the working principle of 4 bit binary adder with carry propagation.	L2
4	Explain multiplexer with the help of logic diagram and corresponding expression.	L2
5	Briefly explain with neat diagram 3:8 decoder.	L2
6	Explain in brief history of HDL and structure of HDL module.	L1
7	Explain the full subtractor with circuit diagram and expression.	L2
8	What is VHDL? show how to model 4:1 MUX using VHDL conditional assignment statement.	L2
9	Using structural model, write VHDL code for Half adder	L2
10	Explain structure of VHDL program. Write VHDL code for 4-bit parallel adder using full adder as component.	L2
11	Explain working of SR latch using NOR gates.	L3
12	Explain with neat diagram, working of JK flip flop and derive the characteristics equation.	L3
13	Derive characteristics equation for the following flip flops i) SR flip flop ii) D flip flop iii) T flip flop iv) JK flip flop	L3

Module Name and Title: 3. Basic structure of computers

Learning Objectives:

At the end of this chapter student should be able to:

1. Explain the meaning and types of functional units of computer.
2. Explain the Stages of bus structure.
3. Explain the Role of performance of clock in processor.
4. Explain the machine instructions and program.
5. Explain different types of addressing modes.

Learning Outcomes:

1. Understanding the meaning and operational concepts.

2. Understanding the Performance of processor clock.
3. Understanding the machine instruction and program.
4. Understanding the instruction and addressing modes.

Lesson Schedule:

Class Number	Portion covered	Book	Page No.
19	Functional Units, Basic Operational Concepts.	T2	2-7
20	Bus structure, Performance – Processor Clock.	T2	9-14
21	Basic Performance Equation, Clock Rate.	T2	14-16
22	Performance Measurement, Machine Instructions and Program.	T2	17-20
23	Memory Location and Addresses.	T2	33-36
24	Memory Operations, Instruction and Instruction sequencing.	T2	36-44
25	Addressing Modes.	T2	48-56

	Questions	Blooms Taxonomy
1	With a neat diagram describe the functional unit of computer.	L1, L2
2	Explain the basic operational concept between processor and memory with neat diagram.	L2
3	Explain various parameters that affects the performance of a computer and also provide the basic performance equation.	L2
4	Explain bus structure.	L2
5	Write a note on processor clock.	L2
6	Explain how to measure the performance of computer.	L2
7	Explain the i) one address instruction ii)two address instruction iii)three address instruction with example?	L2
8	Define byte addressability, Big-Endian and Little-Endian assignment briefly.	L2
9	Explain memory location addressing.	L2
10	Explain memory operation with example.	L2
11	Illustrate instruction and instruction sequential with example.	L2
12	Explain conditional codes with example.	L2
13	Discuss the following addressing modes with example i) Immediate ii) Register iii)Direct iv)Indirect v)Index	L2

Module Name and Title: 4. Input/output Organization

Learning Objectives:

At the end of this chapter student should be able to:

1. Explain the memory mapping and I/O mapping.
2. Explain the need of Interrupt.
3. Explain the Direct Memory Access.
4. Explain the concept of Bus Arbitration.
5. Explain the cache memory and memory mapping.

Learning Outcomes:

1. Understanding the memory mapping and I/O mapping.
2. Understanding the significance of Interrupt.
3. Understanding the concept of Direct memory Access.
4. Understanding the importance of Bus Arbitration.
5. Understanding the concept of cache memory and memory mapping.

Lesson Schedule:

Class Number	Portion covered	Book	Page No.
26	Accessing I/O Devices	T2	204-205
27	Interrupts – Interrupt Hardware	T2	205-210
28,29	Enabling and Disabling Interrupts, Handling Multiple Devices.	T2	211-213
30	Direct Memory Access	T2	234-236
31	Bus Arbitration	T2	237-240
32	Speed, size and Cost of memory systems.	T2	313
33	Cache Memories	T2	313-315
34	Mapping Functions	T2	316-321

	Questions	Blooms Taxonomy
1	Write a note on single bus structure with neat diagram.	L2
2	Explain the concept of memory map I/O and I/O interface with neat diagram.	L1

3	Write a note on i) Interrupt hardware ii) Interrupt nesting.	L2
4	Explain the following i)vector interrupt ii) simultaneous request .	L2
5	Define Interrupt. Point out and explain the various types of enabling and disabling interrupt.	L2
6	Explain the following method of handling interrupt from multiple devices. (i) Diasy chain (ii) Priority structure.	L2
7	Explain operation of DMA with neat diagram.	L2
8	Define Bus arbitration? Explain centralized arbitration mechanism in DMA with a neat diagram.	L2
9	Explain the distributed arbitration mechanism in DMA with a neat diagram.	L2
10	Define cache memory? Explain various types with neat diagram.	L2
11	What is mapping? Explain set associative technique with neat diagram.	L2
12	What is cache memory? Explain direct mapping.	L2

Module Name and Title: 5. Basic Processing Unit

Learning Objectives:

At the end of this chapter student should be able to answer:

1. Explain the fundamental concept of processing unit.
2. Explain the steps in performing ALU operation.
3. Explain how to fetch and store a word in memory.
4. Explain the basic concept of pipelining.
5. Explain the role of cache memory.
6. Explain the pipeline performance.

Learning Outcomes:

1. Understanding the fundamental concepts of processing unit.
2. Understanding the steps in performing ALU operation and register transfer.
3. Understanding how to fetch, store and execution of a word in memory.
4. Understanding the basic concept of pipelining
5. Understanding the role of cache memory
6. Understanding the pipelining performance.

	SES. ENGINEERING COLLEGE, BENGALURU	Form No.: IE/ PP-02/15/01
	Title: Question Paper	

1	M	E			C	S			

Department of Computer Science & Engineering
Internal Assessment Test – I

Subject: Microcontroller
Subject Code: BCS402
Max. Marks: 25
Semester: 4th

Date: 12/06/24
Time: 02:00 pm to 03:00 pm
Duration: 1 Hour
Section: CSE A and B

Note: Answer any two full questions, selected one question from each part

PART A

Sl. No.		Questions	Classification as per Bloom's Taxonomy	CO	Marks Allotted
1	a.	Compare i. Microprocessor and Microcontroller ii. CISC and RISC.	L1	CO1	8
	b.	Discuss the ARM design philosophy.	L2	CO1	4
		OR			
2	a.	With a neat diagram, explain the 4 main hardware components of a ARM based embedded device.	L2	CO1	6
	b.	What is pipelining? Illustrate it with a simple example.	L2	CO1	6

PART B

Sl. No.		Questions	Classification as per Bloom's Taxonomy	CO	Marks Allotted
3	a.	With neat diagram, explain the CPSR	L1	CO1	7
	b.	List and explain ARM processor modes. Also explain ARM core changing from user mode to interrupt request mode on an exception, with neat diagram.	L1	CO1	6
		OR			
4	a.	Explain the different Data processing instruction in ARM.	L1	CO1	8
	b.	Explain the different branch instruction in ARM processor.	L1	CO1	5

Prepared by: Mrs Sneha Jawargi Designation: Assistant Professor Signature:	Approved by: Dr. Mahesh S H Designation: HOD Signature:

M S ENGINEERING COLLEGE
BANGALORE

Title: Scheme of Solution for the 1st Internal Assessment Test
Month and Year: JUNE - 2024.

Subject: Microcontroller
Subject Code: BEC402
Faculty Name: Mrs. Sneha Jewargi

Semester: 4th B.E (CA & B)
Total Marks: 25
Total No. Of Pages:

Q. No	Solution	Marks Distribution
1.a&b	(i) Microprocessor ① It is a processor, memory & I/O components have to connected externally. ② Microprocessor is heart of computer system ③ memory & I/O has to be connected externally, the circuit becomes large. ④ Cannot be used in compact systems & inefficient ⑤ cost is more ⑥ microprocessors do not have power saving system ⑦ Microprocessor are based on von-Neuman model ⑧ Processing speed of general microprocessor is above 1 GHz Microcontroller ① Microcontroller has external processor along with internal memory & I/O components ② Microcontroller is a heart of embedded system. memory & I/O are present internally, the circuit is small. ③ Can be used in compact systems & it is efficient ④ cost is less. ⑤ microprocessors have power saving mode like idle or power saving mode. ⑥ microcontrollers are based on Harvard architecture ⑦ Processing speed of microcontroller is 8 MHz to 50 MHz	4m
	(ii) RISC ① Simple compiler, Complex code generator, Processor ② Simple but powerful instructions ③ Compiler complexity ④ Executes instructions in single cycle ⑤ Instructions are of fixed length ⑥ Large set of general purpose registers ⑦ Any register can contain either data or an address ⑧ Separate load & store instruction ⑨ Transfer data between register & memory CISC ① Compiler, code generator, Processor, Complex ② Instructions are more complicated ③ Too Complex complexity ④ Takes many cycle to execute ⑤ Instructions are of variable length ⑥ Limited set of general purpose registers ⑦ Dedicated registers for specific purpose. ⑧ Mov instruction can be used to transfer between register & memory	4m

Q. No | Solution

1. b. 1. The ARM Processor has been specially designed to be small to reduce power consumption & extend battery operation - application such as mobile phone & personal digital assistants.
2. High code is major requirement since embedded System have limited memory due to cost & physical size restriction. High code density is used for applications that have limited on board memory such as mobile phones.
3. Embedded Systems are price sensitive & use low cost memory devices.
4. ARM has incorporated hardware debug technology within the processor so that software engineers can view what is happening while the processor executing code.
5. For a single-chip solution, the smaller area used by the embedded System processor, the more available space for specialized peripherals.

2. a.

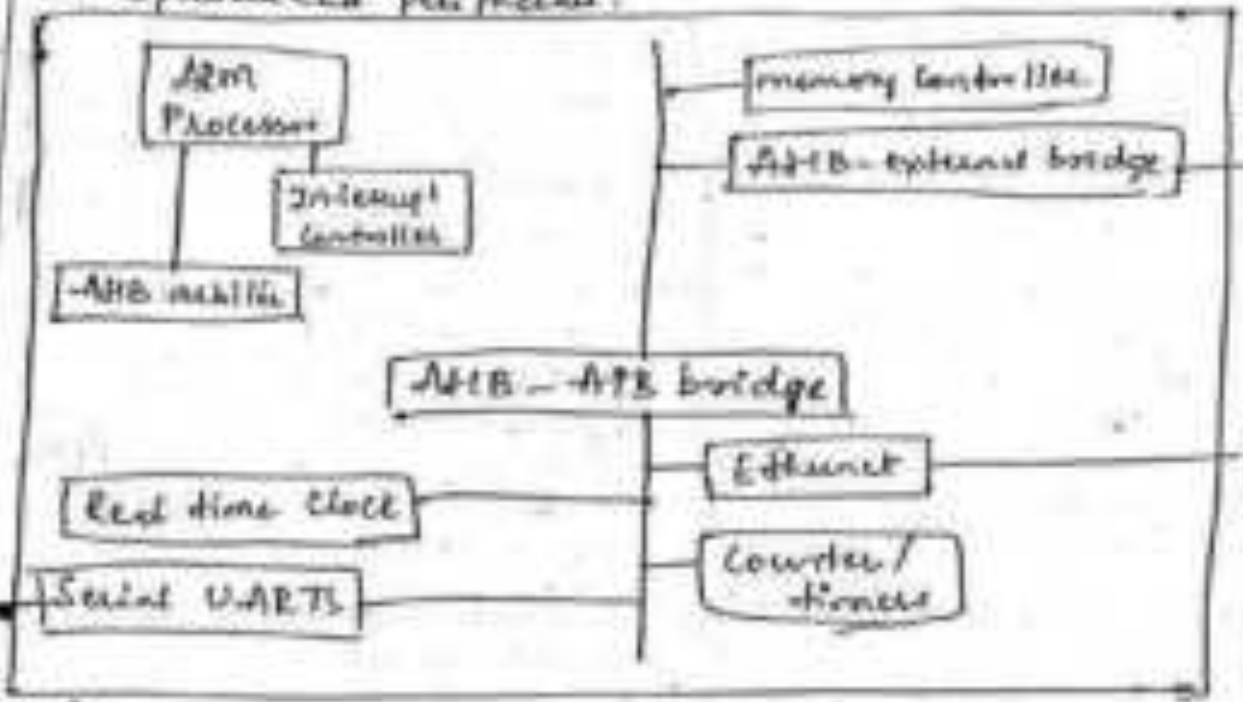


Fig:- ARM - based embedded device, a microcontroller

- The 4 main hardware Components:

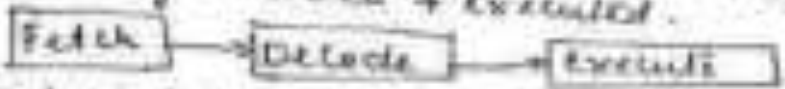
1. ARM Processor :- It controls the embedded device. Different versions of ARM Processor are available to suit the desired operation characteristics. An ARM Processor comprises a core plus surrounding components that interface it with about. These components can include caches +

2. Controllers :- It co-ordinate important functional blocks of system. Two commonly found controllers are interrupt & memory controllers.

3. Peripherals :- It provides all input-output capability external to chip & are responsible for uniqueness of embedded devices.

4. Buses :- It is used to communicate between different parts of device.

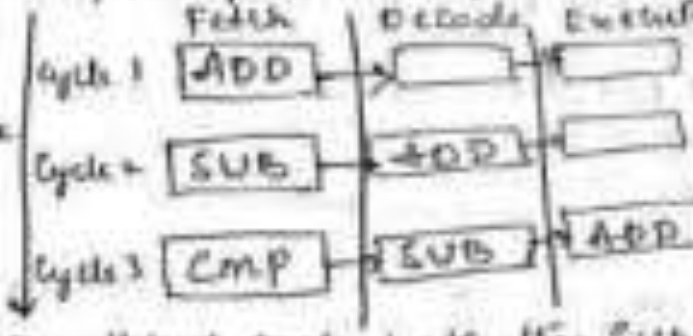
2.6 Pipeline :- A pipeline is the mechanism a RISC processor uses to execute instructions. Using a pipeline speeds up execution by fetching the next instructions while other instructions are being decoded & executed.



Eg: Above Three Stage pipeline

1. Fetch :- fetch loads an instruction from memory.
2. Decode :- Decode identifies the instruction to be executed.
3. Execute :- Execute processes the instruction & writes the result back to a register.

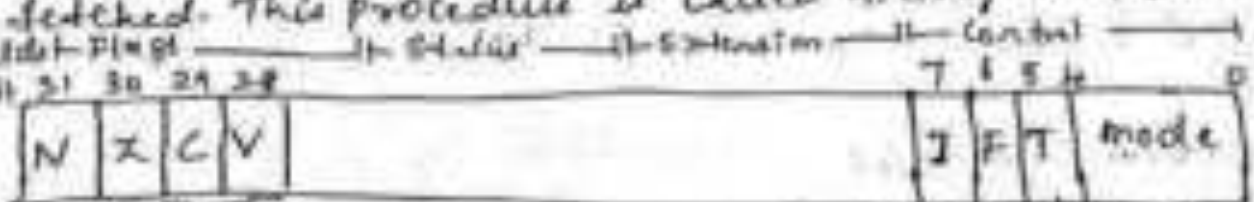
- Three instructions being fetched, decoded & executed by the processor. Each instruction takes a single cycle to complete after the pipeline is filled.



Time

* In the first cycle the core fetches the ADD instruction from memory.
* In second cycle the core fetches the SUB instruction & decodes ADD instruction
* In third cycle, both the SUB & ADD instructions are moved along pipeline. The ADD instruction is executed. the SUB instruction is decoded & CMP instruction is fetched. This procedure is called filling the pipeline.

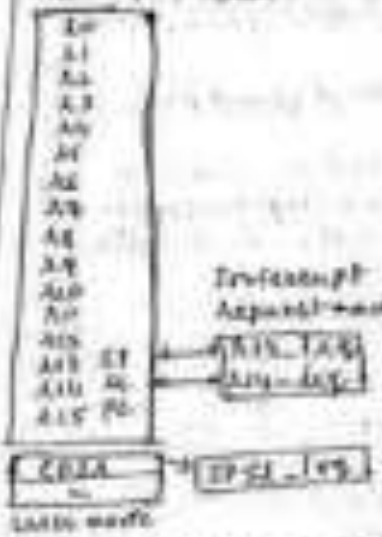
Any



	Control bits
I	IRQ
F	FIQ
T	Thumb

	Flag field
N	Negative from ALU
Z	Zero from ALU
C	Carry
V	Overflow

0	Each executed
J	Jave byte code

Q. No	Solution	Marks Distribution
	Explanation of all processor modes → 7 modes Privileged modes :- Abort, fast interrupt request, interrupt request, supervisor, system, undefined Non-privileged modes :- user	3m = 6m
3. b	ARM Processor modes → 7 modes  	
4. a	Data Processing instructions 1. move instructions - MOV, MVN explanation + one program 2. Barrel Shifter → LSL, LSR, ASR, ROR, RRX → explanation + one program 3. Arithmetic Instructions → ADD, ADC, RSB, RSC, SUB, SBC - explanation + one program 4. Logical Instructions → AND, ORR, EOR, BIC → explanation + one program 5. Comparison instructions → CMN, CMP, TEQ, TST → explanation + one program 6. Multiply instructions → MLA, MUL, SMLAL, SMULL, UMLAL, UMULL → explanation + one program	5m

4. b	Branch instructions
	B, BL, BX, BLX → explanation.
	BL subroutine ; branch to subroutine
	CMP r1, #5 ; compare r1 with 5
	moveq r1, #0 ; if (r1 = 05) then r1 = 0.
	Subroutine
	MOV PC, LR ; return by moving PC = LR
		3m
		+ = 5m
		2m

Prepared by : Mrs. SUCHITA JENNEGI	Approved by : Dr. Mahesh S.H.
Designation : Assistant Professor	Designation : HOD
Signature :	Signature :

	M.S. ENGINEERING COLLEGE, BENGALURU Title: Question Paper	Form No.: R/ PP-02/15/01

1	M	E	2	2	C	S			

Department of Computer Science & Engineering
Internal Assessment Test – II

Subject: Microcontroller
Subject Code: BCS402
Max. Marks: 25
Semester: 4th

Date: 11/07/24
Time: 02:00 pm to 03:30 pm
Duration: 90 minutes
Section: CSE A and B

Note: Answer any two full questions, selected one question from each part

PART A

Sl. No.		Questions	Classification as per Blooms Taxonomy	CO	Marks Allotted
1	a.	Explain briefly the different load store instructions categorized using ARM.	L1	CO1	8
	b.	Discuss swap instruction with an example.	L1	CO1	4
		OR			
2	a.	Explain i. Software interrupts instruction. ii. Program status registers instructions.	L2	CO1	8
	b.	Write a note on loading constants.	L2	CO1	4

PART B

Sl. No.		Questions	Classification as per Blooms Taxonomy	CO	Marks Allotted
3	a.	Explain the basic architecture of cache memory.	L2	CO3	7
	b.	Explain how main memory maps to a cache memory.	L2	CO3	6
		OR			
4	a.	With a neat block diagram explain set associativity cache.	L2	CO3	7
	b.	Briefly explain cache line replacement policies.	L2	CO3	6

Prepared by: Mrs Sneha Jewargi Designation: Assistant Professor Signature:	Approved by: Dr. Mahalesh S H Designation: HOD Signature:

M S ENGINEERING COLLEGE
BANGALORE

Title: Scheme of Solution for the IInd Internal Assessment Test
Month and Year: July – 2024

Subject: Microcontroller
Subject Code: BCS402
Faculty Name: Mrs. SNEHA JEWARGI

Semester: IV-A & B
Total Marks: 25
Total No. Of Pages:

Q. No	Solution	Marks Distribution
1. a. Ans	Load-Store instructions transfer data between memory & processor registers. There are three types of load-store instructions: single-register transfer, multiple register transfer & swap. 1. Single-Register Transfer - LDR, STR, LDRB, STRB, LDRH, STRH, LDRSB, LDRSH 2. Single-Register Load-Store: - Preindex with writeback Addressing mode, Preindex, Postindex 3. Multiple-Register transfer - LDM, STM Addressing mode for load-store: IA, IB, DA, DB Store multiple: - STMIA, STMIB, STMDA, STMDB. Load multiple: - LDMIA, LDMDA, LDMIB, LDMDB 4. Swap Instructions: - SWP, SWPB	each (2m) → (8m).
1.b Ans	Swap Instruction SWP → Swap a word between memory & a register SWPB - Swap a byte between memory & a register Problem - PRE mem32[0x9000] = 0x12345678 r0 = 0x00000000 r1 = 0x11112222 r2 = 0x00009000 SWP r0, r1, [r2]. Post mem32[0x9000] = 0x11112222 r0 = 0x12345678 r1 = 0x11112222 r2 = 0x00009000	(2m) + (4m) (2m)
2.a Ans	(i) Software Interrupt Instructions: - A SWI causes a software interrupt exception, which provides a mechanism for applications to call operating system routines. SWI → software interrupt — lr_svc = address of instruction following SWI spsr_svc = cpsr pc = vectors + 0x8 cpsr mode = SVC cpsr I = 1 (mask IRQ interrupts)	(4m) +

Q.No	Solution	Marks Distribution

PRE CPSR: nzcvqjft_USER
PC = 0x00000000
LR = 0x14
R0 = 0x12
0x00000000 SUB R0,R0,R0

POST CPSR: nzcvqjft_SVC
SPSR: nzcvqjft_USER
PC = 0x00000008
LR = 0x00000004
R0 = 0x12

(iii) Program Status Register Instructions

MRS - Copy Program status register to general purpose register
MSR - move a general purpose register to program status register
MSR - move an immediate value to program status register.

PRE CPSR: nzcvqjft_SVC
MRS R1, CPSR
BIC R1, R1, #0x80
MSR CPSR_c, R1
POST CPSR: nzcvqjft_SVC

Coprocessor instructions
CDP — Coprocessor data processing
MRC MCR — Coprocessor register transfer
LDC STC — Coprocessor memory transfer

2.bAns Loading Constants
LDR - Load Constant Pseudoinstruction
ADR - Load address Pseudoinstruction

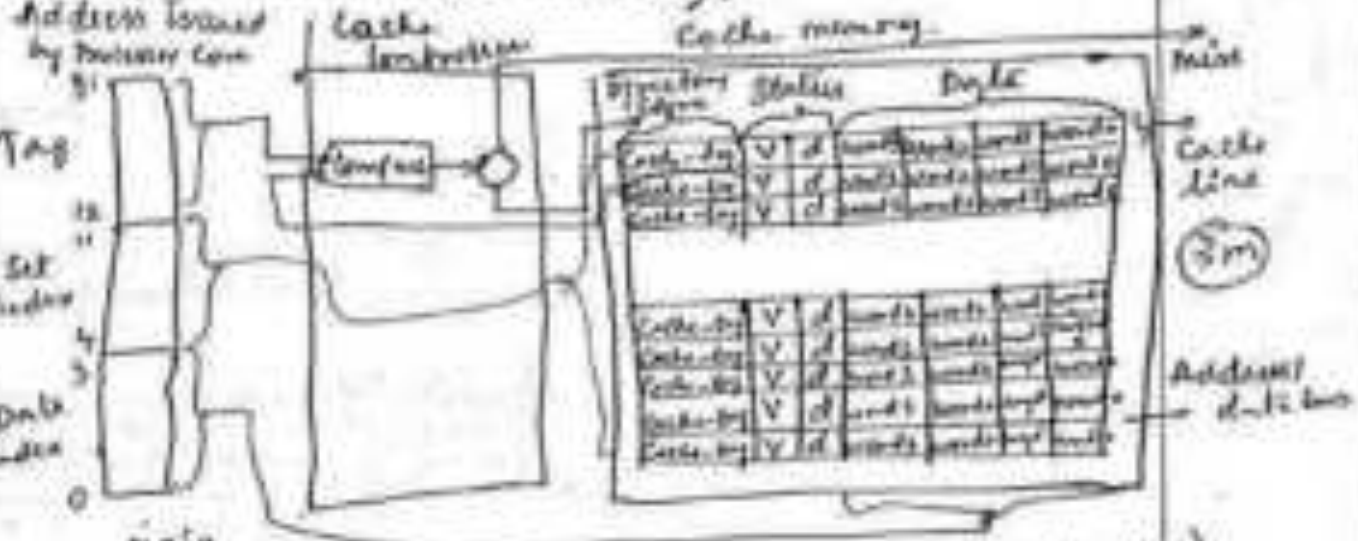
Pseudoinstruction	Actual instruction
LDR R0, =0x FF	mov R0, #0x FF
LDR R0, =0x55555555	LDR R0, [PC, #offset_12]

PRE none----
MVN R0, #0x00000000
POST R0 = 0xFFFFFFFF

3.bAns It has three main parts:- a directory Store, a data section & Status Information
* Cache uses a directory Store to hold the address identifying where cache line was copied from main memory. The directory entry is known as cache tag.

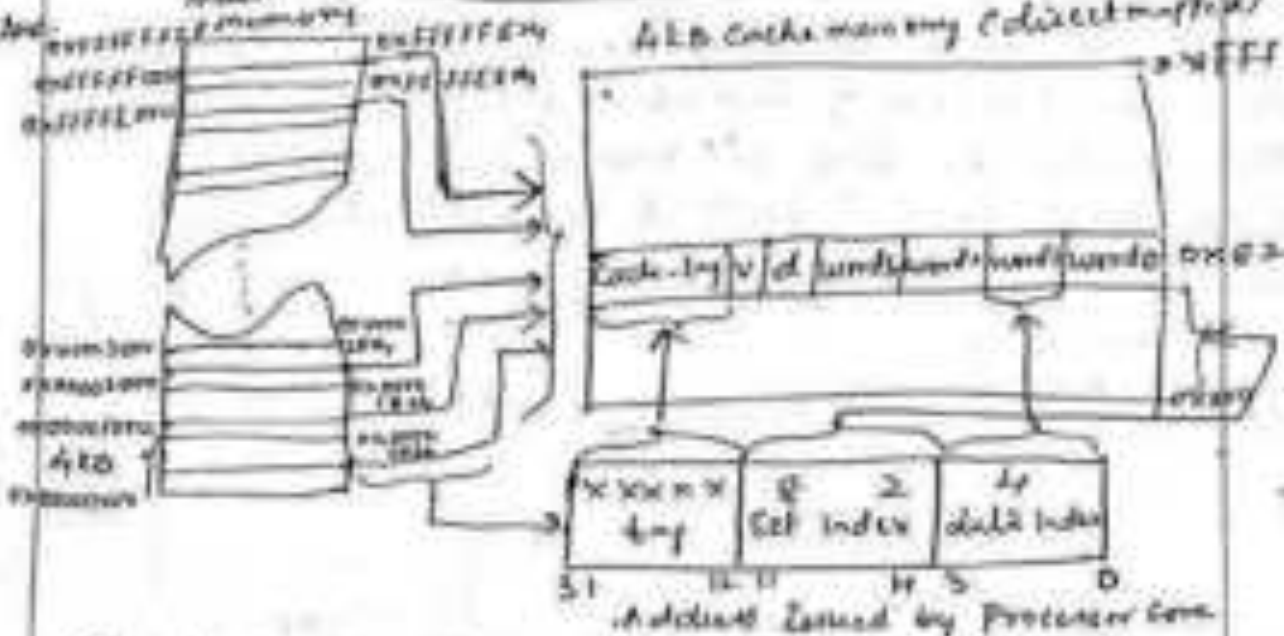
Solution	Marks Distribution

- Two common status bits are valid bit & dirty bit.
- valid bit marks a cache line as active, meaning it contains live data originally taken from main memory.
- A dirty bit defines whether or not a cache line contains data that is different from the value it represents in main memory. (1m)



(3m)

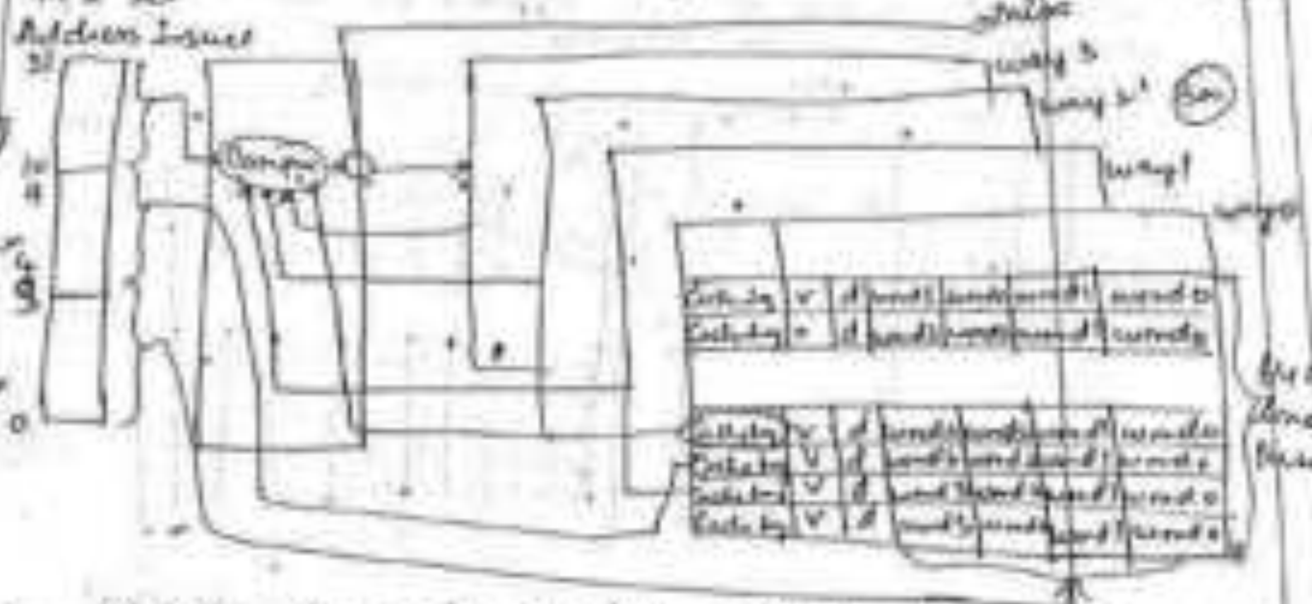
3 blocks



(3m)

+ = (7m)

- The data index selects word/halfword/byte in cache line, in this case the second word in cache line (4m)
- Explanation of Data Streaming, eviction, thrashing

Q. No	Solution	Marks Distribution
b Ans	Set of cache lines pointed by set index – set associative. Data & code from main memory allocated in 4 way in a set	explanation (2m) + (3m)
		(5m)
c Ans	The cache line for replacement is known as victim. The process of selecting & replacing a victim in cache line is known as eviction. ARM cached core support 2 replacement policies ① Round-robin or cyclic replacement – explanation ② Pseudorandom replacement – explanation	(3m) (2m) (6m) (2m)

Prepared by : Ms. Sneha Jewargi
Designation : Assistant Professor
Signature : Sneha

Approved by : Dr. Mallesh. S.H
Designation : HOD
Signature :

	M.S. ENGINEERING COLLEGE, BENGALURU	Form No.: IE/ PP-02/18-01
	Title: Question Paper	

1	M	E	2	2	C	S			

Department of Computer Science & Engineering
Internal Assessment Test – III

Subject: Microcontroller
Subject Code: BCS482
Max. Marks: 25
Semester: 4th

Date: 05/08/24
Time: 02:00 pm to 03:30 pm
Duration: 90 minutes
Section: CSE A and B

Note: Answer any two full questions, selected one question from each part

PART A

Sl. No.		Questions	Classification as per Bloom's Taxonomy	CO	Marks Allotted
3	a.	Explain the function argument types and explain with an example using C-CODE, GCC examples and arrays examples.	L2	CO3	6
	b.	Discuss how registers are allocated to optimize the program.	L3	CO3	4
		OR			
4	a.	Explain the ATPCS registration passing with example of using register passing.	L2	CO3	6
	b.	Explain pointer aliasing and write a code for function increment two integer values by 2 using pointers.	L2	CO3	6

PART B

Sl. No.		Questions	Classification as per Bloom's Taxonomy	CO	Marks Allotted
3	a.	Explain with a neat diagram ARM processor exceptions and modes.	L2	CO4	7
	b.	Explain the exception priority levels.	L2	CO4	6
		OR			
4	a.	Explain assigning interrupts and interrupt latency.	L2	CO4	7
	b.	Explain what happens when an IRQ and FIQ exception is raised with an ARM processor.	L2	CO4	6

Prepared by: Mrs Sneha Jowargi Designation: Assistant Professor Signature:	Approved by: Dr. Malabala S H Designation: HOD Signature:

M S I M INEERING COLLEGE
BANGALORE

Title: Scheme of Solution for Internal Assessment Test
Month and Year: Aug - 2019

Subject: Microcontroller
Subject Code: BCS402
Faculty Name: Mrs. Sneha Tewargi

Semester: 4th A & B
Total Marks: 25
Total No. Of Pages:

Q. No	Solution	Marks Distribution

10. a) Short add_v1 (short a, short b)
{
return a + (b>>1);
}

- The input values a, b & the return value will be stored in 32 bit ARM registers
- ARM C compiler explanation.

```
add_v1
    ADD  r0, r0, r1, ASR #1 ; r0 = (int)a + ((int)b>>1)
    mov  r0, r0, LSL #16 ;
    mov  r0, r0, ASR #16 ; r0 = (short)r0
    mov  PC, r14         ; return r0
```

- ARM GCC compiler explanation

```
add_v1_gcc
    mov  r0, r0, LSL #16
    mov  r2, r1, LSL #16
    mov  r1, r1, ASR #17   ; r1 = (int)b>>1
    ADD  r1, r1, r0, ASR #16 ; r1 = (int)a
    mov  r1, r1, LSL #16
    mov  r0, r1, ASR #16   ; r0 = (short)r1
    mov  PC, r14           ; return r0.
```

(6m)

(2m)

(2m)

4 marks

b) ARM Thumb procedure call standard (ATPCS) which is used in code generated by C compiler.

Register number	Alternate register names	ATPCS register usage
r0	a1	Argument register: holds the first four function arguments on a function call & the return value on a function return
r1	a2	
r2	a3	
r3	a4	
r4	v1	
r5	v2	
r6	v3	
r7	v4	
r8	v5	

(6m)

+

Q. No.	Solution	Marks Distribution

R9	V6 SB	General variable register - R9 holds the static base address
R10	V7 SL	General variable register - R10 holds stack limit address
R11	V8 FP	General variable register. Hence uses a frame pointer
R12	IP	General scratch register that the function can corrupt
R13	SP	Stack pointer, full descending stack
R14	LR	Link register, holds return address
R15	PC	Program counter

(6M)

Explanation ——— (2M)

— (1m)

```
typedef struct {
  char *Q_start;
  char *Q_end;
  char *Q_ptr;
} Queue;
void queue_bytes_v2(
  Queue *queue, char *data,
  unsigned int N)
{
  char *Q_ptr = queue->Q_ptr;
  char *Q_end = queue->Q_end;
  do
  {
    *(Q_ptr++) = *(data++);
    if (Q_ptr == Q_end)
    {
      Q_ptr = queue->Q_start;
    }
  } while (--N);
  queue->Q_ptr = Q_ptr;
}
```

(3M) 6m

```
queue_bytes_v2          ; save lr on stack
  STR  r14,[r13,#-4]!
  LDR  r3,[r0,#8]       ; r3 = queue->Q_ptr
  LDR  r14,[r0,#4]      ; r14 = queue->Q_end
queue_v2_loop
  LDRB r12,[r1],#1      ; r12 = *(data++)
  STRB r12,[r3],#1
  CMP  r3,r14
  LDREQ r3,[r0,#0]
  SUBS r2,r2,#1
  BNE  queue_v2_loop    ; if (--N != 0) goto loop
  STR  r3,[r0,#8]       ; queue->Q_ptr = r3
  LDR  pc,[r13],#4      ; return
```

(3M)

Q no.	Solution	Marks Distribution
5b.	Two pointers are said to be alias when they point to the same address. If you write to one pointer, it will reflect the value you read from the other pointer.	1m

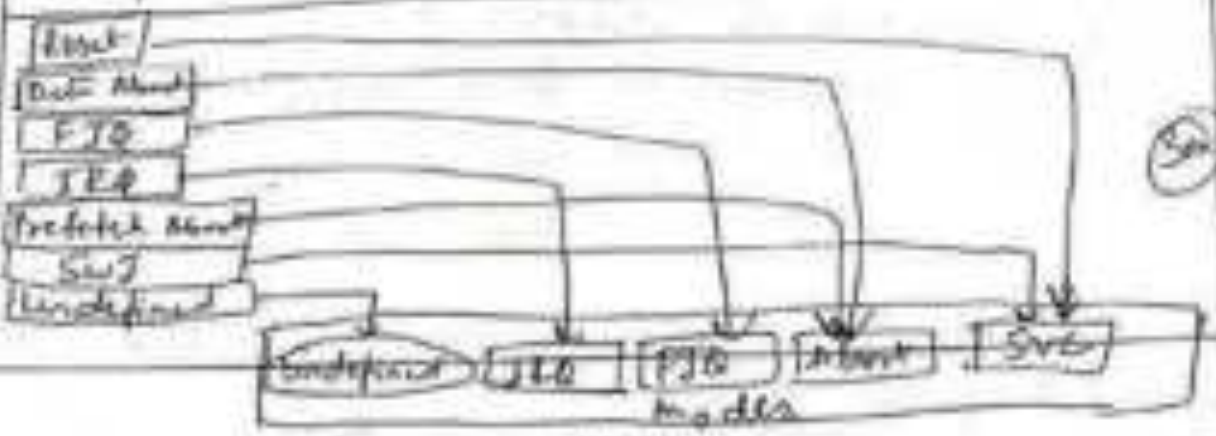
	function increments two times values by step amount
	Void times_V1 (int *time1, int *time2, int *step)
	{
	*time1 += *step;
	*time2 += step;
	}
	Compiles to
	times_V1
	LDR R3,[R0 #0] ; R3 = *time1
	LDR R12,[R2, #0] ; R12 = *step
	ADD R3, R3, R12 ; R3 += R12
	STR R2,[R0, #0] ; *time1 = R3
	LDR R0,[R1, #0] ; R0 = *time2
	LDR R2,[R2, #0] ; R2 = *step
	ADD R0, R0, R2 ; R0 += R2
	STR R0,[R1, #0] ; *time2 = R0
	mov PC, R14 ; return
		1m
		4m
		1m

3a.	Non Processor modes can be entered manually by changing CPSR. when an exception occurs it mode change, it will save automatically ① Saves the CPSR to SPSR of exception mode ② Saves the PC to LR of exception mode	2m

Exception mode	mode	main purpose
Fast interrupt request	FIQ	fast interrupt request handling
Interrupt request	IRQ	interrupt request handling
SWI & Reset	SVC	Protected mode for OS
Prefetch abort & Data Abort	Abort	virtual memory & memory protection handling
undefined instruction	undefined	Software emulation of hardware in processors

2m

7m

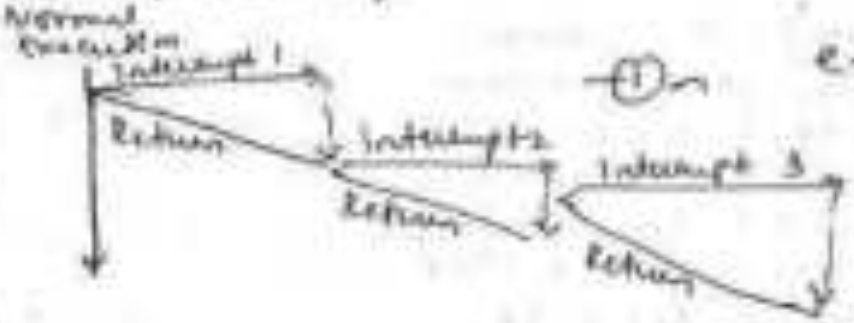


3m

Page No.

Q. No	Solution	Marks Distribution

4a. Ans: Assigning interrupt: Explanation of
(1) Software interrupts
(2) Interrupt requests
(3) Fast interrupt requests } 3m
Interrupt latency



1m explanation 2m

3m

4b. Ans: IRQ & FIQ exceptions only occurs when a specific interrupt mask is cleared in CPSR. The ARM processor will continue executing the current instruction in execution stage of pipeline before handling interrupt

1. The processor changes to a specific interrupt request mode, which reflects the interrupt being raised.
2. Previous mode CPSR is saved into SPSR of new interrupt request mode
3. PC is saved in LR of new interrupt request mode.
4. Interrupts are disabled. either of IRQ or both IRQ & FIQ exception are disabled.
5. The processor branches to specific entry in vector table

Prepared by: Mrs. Sneha Jennagi	Approved by: Dr. Malatesh. S H
Designation: Assistant Professor	Designation: HOD
Signature: Sneha	Signature:

	M.S. ENGINEERING COLLEGE Bengaluru
	Department of Computer Science & Engineering
	Title: Internal Examination Circular

Date: 13-01-2024

CIRCULAR

All Staff members are hereby requested to submit the **Question Papers and Scheme of Evaluation** for the **First Internal Assessment (for 5th Semester)** on or before 16/01/2024. The First IA is scheduled on 17th, 18th and 19th of January 2024.

Sl. No.	Faculty Name	Signature with Date
1	Mrs. Bhagya M.	
2	Mrs. Dipti Patnayak	Dipti 14/01/24
3	Mrs. Prabha Naik	
4	Ms. Aishwarya M.	
5	Mrs. Shwetha K.S.	
6	Mrs. Shwetha K.S.	

Prepared by: Mrs. Dipti Patnayak Designation: Test Coordinator Signature: Dipti	Approved by: Dr. Mahesh S.H. Designation: HOD Signature:

	M.S. ENGINEERING COLLEGE BENGALURU Title: Internal Assessment Time Table	Form No. : R/ PP-02/13/ 01
	Department : CSE Semester: V	Date : 13/01/2024 Test No. : 1ST

V Semester 2021 Scheme

Date	Subject Code	10.00 AM to 11.30 AM	Subject Code	02.00 PM to 03.30 PM
17/01/2024	21CS51	Automata Theory & Compiler Design	21CS52	Computer Networks
18/01/2024	21CS53	Database Management Systems	21CIV57	Environmental Studies
19/01/2024	21AI54	Artificial Intelligence & Machine Learning	21RMI56	Research Methodology & Intellectual Property Rights

Prepared By : Mrs. Dipti Patnayak	Approved By : Dr. Malatesh S.H.	Verified By : Dr. P Mahadevaswamy
Designation : Associate Professor	Designation : HOD	Designation : Principal
Signature: Dipti	Signature:	Signature:

	M.S. ENGINEERING COLLEGE BENGALURU Title: Internal Assessment Time Table	Form No. : R/ PP-02/13/ 01
	Department : CSE Semester: V	Date : 13/02/2024 Test No. : 2nd

V Semester 2021 Scheme

Date	Subject Code	10:00 AM to 11:30 AM	Subject Code	12:00 PM to 01:30 PM
14/02/2024	21CS53	Database Management Systems	21CS52	Computer Networks
15/02/2024	21AI54	Artificial Intelligence & Machine Learning	21RM56	Research Methodology & Intellectual Property Rights
16/02/2024	21CS51	Automata Theory & Compiler Design	21CIV57	Environmental Studies

Prepared By : Mrs. Dipti Patnayak Designation : Associate Professor Signature: Dipti	Approved By : Dr. Malatesh S.H. Designation : HOD Signature:	Verified By : Dr. P Mahadevaswamy Designation : Principal Signature:

	M.S. ENGINEERING COLLEGE BENGALURU Title: Internal Assessment Time Table	Form No. : R/ PP-02/13/ 01

Department : CSE
Semester: V

Date : 07/03/2024
Test No. : 3rd

V Semester 2021 Scheme

Date	Subject Code	10:00 AM to 11:30 AM	Subject Code	02:00 PM to 03:30 PM
11/03/2024	21CS51	Automata Theory & Compiler Design	21CS52	Computer Networks
12/03/2024	21CS53	Database Management Systems	21CAI54	Artificial Intelligence & Machine Learning
13/03/2024	21RMI56	Research Methodology & Intellectual Property Rights	21CIV57	Environmental Studies

Prepared By : Mrs. Dipti Patnayak	Approved By : Dr. Malatesh S.H.	Verified By : Dr. P Mahadevaswamy
Designation : Associate Professor	Designation : HOD	Designation : Principal
Signature: Dipti	Signature:	Signature:

	M.S. ENGINEERING COLLEGE BENGALURU Title: Internal Assessment Time Table	Form No. : R/ PP-02/13/ 01
	Department : CSE Semester: V	Date : 13/01/2024 Test No. : 1ST

V Semester 2021 Scheme

Date	Subject Code	10.00 AM to 11.30 AM	Subject Code	02.00 PM to 03.30 PM
17/01/2024	21CS51	Automata Theory & Compiler Design	21CS52	Computer Networks
18/01/2024	21CS53	Database Management Systems	21CIV57	Environmental Studies
19/01/2024	21AI54	Artificial Intelligence & Machine Learning	21RMI56	Research Methodology & Intellectual Property Rights

Prepared By : Mrs. Dipti Patnayak	Approved By : Dr. Malatesh S.H.	Verified By : Dr. P Mahadevaswamy
Designation : Associate Professor	Designation : HOD	Designation : Principal
Signature: Dipti	Signature:	Signature:

	M.S. ENGINEERING COLLEGE BENGALURU Title: Internal Assessment Time Table	Form No. : R/ PP-02/13/ 01
	Department : CSE Semester: V	Date : 13/02/2024 Test No. : 2nd

V Semester 2021 Scheme

Date	Subject Code	10:00 AM to 11:30 AM	Subject Code	12:00 PM to 01:30 PM
14/02/2024	21CS53	Database Management Systems	21CS52	Computer Networks
15/02/2024	21AI54	Artificial Intelligence & Machine Learning	21RM56	Research Methodology & Intellectual Property Rights
16/02/2024	21CS51	Automata Theory & Compiler Design	21CIV57	Environmental Studies

Prepared By : Mrs. Dipti Patnayak Designation : Associate Professor Signature: Dipti	Approved By : Dr. Malatesh S.H. Designation : HOD Signature:	Verified By : Dr. P Mahadevaswamy Designation : Principal Signature:

	M.S. ENGINEERING COLLEGE BENGALURU Title: Internal Assessment Time Table	Form No. : R/ PP-02/13/ 01

Department : CSE
Semester: V

Date : 07/03/2024
Test No. : 3rd

V Semester 2021 Scheme

Date	Subject Code	10:00 AM to 11:30 AM	Subject Code	02:00 PM to 03:30 PM
11/03/2024	21CS51	Automata Theory & Compiler Design	21CS52	Computer Networks
12/03/2024	21CS53	Database Management Systems	21CAI54	Artificial Intelligence & Machine Learning
13/03/2024	21RMI56	Research Methodology & Intellectual Property Rights	21CIV57	Environmental Studies

Prepared By : Mrs. Dipti Patnayak	Approved By : Dr. Malatesh S.H.	Verified By : Dr. P Mahadevaswamy
Designation : Associate Professor	Designation : HOD	Designation : Principal
Signature: Dipti	Signature:	Signature:

SES ENGINEERING COLLEGE
BENGALURU

Form No.:
IU/PP-02/14/01

Title: Attendance & Room Superintendent's Report

Semester :V | Room No :LH-108

Dept.: CSE

Third Internal Assessment Test Attendance Details

Sl. No.	STUDENT NAME	USN	DATE :- 12/03/24 TIME :- 10:00 am 11:30 am SUB/EXT:- ATC (21CS52)	12/03/24 10:00 am 11:30 am 02:00 pm 03:30 pm CN (19CS52)	12/03/24 10:00 am 11:30 am DBMS (21CS53)	12/03/24 02:00 pm 03:30 pm AI (21AI56)	13/03/24 10:00 am 11:30 am RMI (21RMI56)	13/03/24 02:00 pm 03:30 pm CIV (21CIV57)	Signature of the student
1	ABANISHWA	1MS21CS001	P	P	P	P	P	P	
2	ADARSH R	1MS21CS001	P	P	P	P	P	P	
3	AFREEN A	1MS21CS003	P	P	P	P	P	P	
4	AMAN KUMAR	1MS21CS004	P	P	P	P	P	P	
5	ANIRUDHA J	1MS21CS006	P	P	P	P	P	P	
6	ANJALI KUMARI	1MS21CS007	P	P	P	P	P	P	
7	ANKIT B.M.	1MS21CS008	P	P	P	P	P	P	
8	ARCHANA A	1MS21CS009	P	P	P	P	P	P	
9	ARVIND G	1MS21CS010	P	P	P	P	P	P	
10	AYUSH VISHWAKARMA K	1MS21CS012	P	P	P	P	P	P	
11	BASAVARAJA S	1MS21CS013		P	P	P	P	P	
12	BHAVYA B	1MS21CS014	P	P	P	P	P	P	
13	BIKASH KUMAR SINGH	1MS21CS015	P	P	P	P	P	P	
14	BRAHANI KUMAR SAH	1MS21CS017	P	P	P			P	
15	CHANDAN B M	1MS21CS018	P	P	P	P	P	P	
16	CHANDAN B R	1MS21CS019	P	P	P	P	P	P	
17	CHANDANA K S	1MS21CS020		P	P	P	P	P	
TOTAL No. OF STUDENTS PRESENT :									
TOTAL No. OF STUDENTS ABSENT :									
ROOM SUPERINTENDENT NAME & SIGNATURE WITH DATE :									
USNs (Candidates b/s Malpractice)									
SQUAD SIGNATURES									

Verified By : Mrs. Dipti Jaiswal
Designation : Test Coordinator
Signature :

Approved By : Dr. Mahesh S.H.
Designation : HOD
Signature :

M.S. ENGINEERING COLLEGE
BENGALURU

Title: Attendance & Room Superintendent's Report

Dept. : CSE | Semester : V | Room No. : CH-[illegible]

Third Internal Assessment Test Attendance Details

Sl. No.	STUDENT NAME	USN	ATC	CN	DBMS	AI	RMI	CIV	Signature of students
1	CHANDRA [illegible]	[illegible]	P	P	P	P	P	P	Chan[illegible]
2	[illegible]	[illegible]	P	P	P	P	P	P	Dichh[illegible]
3	DEVIKA [illegible]	[illegible]	P	P	P	P	P	P	Devika
4	[illegible]	[illegible]	P	P	P	P	P	P	[illegible]
5	[illegible]	[illegible]	P	P	P	P	P	P	Dhanush M
6	[illegible]	[illegible]	P	P	P	P	P	P	[illegible]
7	DIVYA RANI [illegible]	[illegible]	P	P	P	P	P	P	Divya
8	GAGANA [illegible]	[illegible]	P	P	P	P	P	P	[illegible]
9	GANAVI C	[illegible]	P	P	P	P	P	P	Ganavi C
10	HARSHITHA PADMAVATHI	[illegible]	P	P	P	P	P	P	[illegible]
11	[illegible]	[illegible]	P	P	P	P	P	P	[illegible]
12	ESHWARI	[illegible]	P	P	P	P	P	P	Eshwari
13	JYOTHI PATIL	[illegible]	P	P	P	P	P	P	Jyothi
14	KAVANA [illegible]	[illegible]	P	P	P	P	P	P	Kavana.S
15	KOMAL A	[illegible]	P	P	P	P	P	P	[illegible]
16	SAI CHAITANYA	[illegible]							
17	L C SRUSTI	[illegible]	P	P	P	P	P	P	L.G.Srusti
TOTAL No. OF STUDENTS PRESENT :									
TOTAL No. OF STUDENTS ABSENT :									
ROOM SUPERINTENDENT NAME			[illegible]	[illegible]	Rachana	Nagu	Preethi	Suma	
USNs (Candidates in Malpractice)									
SQUAD SIGNATURES									

Verified By : Mrs. [illegible] Pattanayak
Designation : Test Coordinator
Signature : [illegible]

Approved By : Dr. Malatesh S.H.
Designation : HOD
Signature :

M.S. ENGINEERING COLLEGE
BENGALURU

Title: Attendance & Room Superintendent's Report

Form No.: R/
PP-02/ 14/ 01

Semester : V | Room No : LH-116/107

Dept. : CSE

Third Internal Assessment Test Attendance Details

Sl. No.	STUDENT NAME	DATE : TIME : SUBJECT : USN	13/9/24 10:00 am - 11:30 am ATC (21CS51)	13/9/24 02:00 pm - 03:30 pm CN (21CS52)	12/9/24 10:00 am - 11:30 am BDMS (21CS53)	12/9/24 02:00 pm - 03:30 pm AI (21AI54)	13/9/24 10:00am - 11:30am RMI (21RMI56)	13/9/24 02:30 pm - 03:30 pm CIV (21CIV57)	Signature of the student
1	MD SALMAN KHAN	1MS21CS039	P	P	P	P	P	P	
2			P	P	P	P	P	P	
3			P	P	P	P	P	P	
4			P	P	P	P	P	P	
5			P	P	P	P	P	P	
6			P	P	P	P	P	P	
7				P	P	P	P	P	
8			P	P	P	P	P	P	
9			P	P	P	P	P	P	
10			P	P	P	P	P	P	
11			P	P	P	P			
12									
13			P	P	P	P	P	P	
14			P	P	P	P	P	P	
15			P	P	P	P	P	P	
16					P	P	P	P	
17	PANDYA PRANAV	1MS21CS055	P	P	P	P	P	P	
TOTAL No. OF STUDENTS PRESENT :									
TOTAL No. OF STUDENTS ABSENT :									
ROOM SUPERINTENDENT NAME & SIGNATURE WITH DATE :									
USNs (Candidates b/s Malpractice)									
SQUAD SIGNATURES									

Verified By : Mrs. Dipti Pereyra
Designation : Test Coordinator
Signature :

Approved By : Dr. Mahendra S.H.
Designation : HOD
Signature :

PP-[illegible]

M.S. ENGINEERING COLLEGE
BENGALURU

Title: Attendance & Room Superintendent's Report

Dept.: CSE | Semester: V | Room No: LH-107

Third Internal Assessment Test Attendance Details

Sl. No.	STUDENT NAME	DATE: / TIME: / SUBJECT: / USN	ATC (21CS51)	CN (21CS52)	DBMS (21CS53)	AI (21AI54)	RMI (21RM[illegible])	CIV (21CIV57)	Signature of the student
		DATE:	[illegible]		12/03/24		13/03/24		
		TIME:	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
1	PAVAN VENKATESH GUDDA	[illegible]	P	P	P	P	P	P	
2	PRAGATI PALAKSHAPPA	[illegible]	P	P	P	P	P	P	
3	PRATHIKSHA GOPAL	[illegible]	P	P	P	P	P	P	
4	PRATEEK C S	[illegible]	P		P		P	P	
5	PREETHAM K S	[illegible]	P	P	P	P	P	P	
6	PRASHANTH KUMAR H R	[illegible]	P	P	P	P	P	P	
7	PRIYA K R	[illegible]	P	P	P	P	P	P	
8	PRIYANKA N R	[illegible]	P	P	P	P			
9	PUNEETH R	[illegible]	P				P	P	
10	PUNEETHRAJ M B	[illegible]	P	P	P	P	P	P	
11	RAGHUNANDAN	[illegible]	P	P	P	P	P	P	
12	RAJAN GUPTA	[illegible]	P	P	P	P	P	P	
13	RAKESH	[illegible]	P	P	P	P	P	P	
14	RAKSHIT M S	[illegible]							
15	RAMESH T A	[illegible]	P	P	P	P	P	P	
16	RAMYA R	[illegible]	P	P	P	P	P	P	
17	RANA SATISHRAO	[illegible]	P	P	P	P	P	P	
TOTAL No. OF STUDENTS PRESENT :									
TOTAL No. OF STUDENTS ABSENT :									
ROOM SUPERINTENDENT NAME SIGNATURE WITH DATE :									
USNs (Candidates b/w Malpractice)									
SQUAD SIGNATURES									

Verified By : Mrs. Dipti Pattnayak
Designation : Test Coordinator
Signature :

Approved By : Dr. Mahesh S.R.
Designation : HOD
Signature :

[logo]	**M.S. ENGINEERING COLLEGE BENGALURU**	Form No.: RU FP-02/14/01
	Title: Attendance & Room Superintendent's Report	

Semester : V | Room No : LH-107

Dept. : CSE

Third Internal Assessment Test Attendance Details

Sl. No.	STUDENT NAME	DATE →	11/03/24		12/03/24		13/03/24		Signature of the student
		TIME →	10:00 am 11:30 am	02:00 pm 03:30 pm	10:00 am 11:30 am	02:00 pm 03:30 pm	10:00am 11:30am	02:00 pm 03:30 pm	
		SUBJECT → / USN	ATC (21CS51)	CN (21CS52)	DBMS (21CS53)	AI (21AI54)	RMS (21RMI56)	CIV (21CIV57)	
1	RITIK KUMAR GAUTAM	[illegible]	P	P	P	P	P	P	[signature]
2	ROHITH G A	[illegible]	P		P	P	P	P	[signature]
3	RUCHITHA G S	[illegible]	P	P	P	P	P	P	[signature]
4	S ABZAL A	[illegible]	P	P	P	P	P	P	[signature]
5	SAI DEEPAK Y	[illegible]	P	P	P	P	P	P	[signature]
6	SAI DHANUSH S M	[illegible]	P	P	P	P	P	P	[signature]
7	SANDHYA B M	[illegible]							
8	[illegible]	[illegible]	P	P	P	P	P	P	[signature]
9	SHEIK SHOAIB AKTHAR	[illegible]	P	P	P	P	P	P	[signature]
10	SHIV KUMAR YADAV	[illegible]	P	P	P	P	P	P	[signature]
11	SHOBHITHA S R	[illegible]	P	P	P	P	P	P	[signature]
12	SHRAVAN KUMAR	[illegible]	P	P	P	P	P	P	[signature]
13	[illegible]	[illegible]	P	P	P	P	P	P	[signature]
14	[illegible] KATTIMANI	[illegible]	P	P	P	P	P	P	[signature]
15	SHREYA VEERABASAPPA KABADE	[illegible]	P	P	P	P	P	P	[signature]
16	SHUBHAM KUMAR	[illegible]	P	P	P	P	P	P	[signature]
17	SPOORTHI ARAGANJI	[illegible]	P	P	P	P	P	P	[signature]
TOTAL No. OF STUDENTS PRESENT :									
TOTAL No. OF STUDENTS ABSENT :									
ROOM SUPERINTENDENT NAME & SIGNATURE WITH DATE :			[signature]	[signature]	[signature]	[signature]	[signature]	[signature]	
USNs (Candidates b/o Malpractice)									
SQUAD SIGNATURE									

Scrutinized by: [illegible]
Designation: Test coordinator
Signature: [signature]

Approved by: [illegible]
Designation: HOD
Signature: [signature]

M.S. ENGINEERING ...
BENGALURU
Title: Attendance & Room Superintendent's Report

Semester : V | Room No : ...

Dept. : CSE

Third Internal Assessment Test Attendance Details

Sl. No.	STUDENT NAME	USN	ATC (21CS51)	CN (21CS52)	DBMS (21CS53)	AI (21AI54)	RM (21RMI56)	CIV (21CIV57)	SIGNATURE
1	SRI HARI G R	[illegible]	P	P	P	P	P	P	[signature]
2	SUDARSHAN BABU H	[illegible]	P	P	P	P	P	P	[signature]
3	SUDARSHAN B	[illegible]	P		P	P			[signature]
4	SUDEEP S	[illegible]	P	P	P	P	P	P	[signature]
5	SUPRIYA	[illegible]	P	P	P	P	P	P	[signature]
6	... GOWDA R K	[illegible]	P	P	P	P	P	P	[signature]
7	SUNIL ...	[illegible]	P	P	P	P	P	P	[signature]
8	SUNIL KUMAR	[illegible]	P	P	P	P	P	P	[signature]
9	SUPRIYA	[illegible]	P	P	P	P	P	P	[signature]
10	SUSHMA B M	[illegible]	P	P	P	P	P	P	[signature]
11	SUSMITHA K	[illegible]							
12	TEJASWINI G T	[illegible]	P	P	P	P	P	P	[signature]
13	TILAK ... NAIK	[illegible]	P	P	P	P	P	P	[signature]
14	UDAY B	[illegible]	P	P	P	P	P	P	[signature]
15	UPPARA SIDDARTH	[illegible]	P	P	P	P	P	P	[signature]
16	VAISHNAVI A P	[illegible]	P	P	P		P	P	[signature]
17	VANSHITHA	[illegible]	P	P	P	P	P	P	[signature]
TOTAL No. OF STUDENTS PRESENT :									
TOTAL No. OF STUDENTS ABSENT :									
ROOM SUPERINTENDENT NAME & SIGNATURE WITH DATE :			[signature]	[signature]	[signature]	[signature]	[signature]	[signature]	
USNs (Candidates b/o Malpractice)									
SQUAD SIGNATURES									

Verified By : Mrs. Dipti Patnayak
Designation : Test Coordinator
Signature with date : [signature]

Approved By : Dr. Mahesh S.H.
Designation : HOD
Signature with date : [signature]

M.S. ENGINEERING COLLEGE
BENGALURU

Form No.: IE/
PP-02/ 14/ 01

Title: Attendance & Room Superintendent's Report

Semester : V | Room No : LH-105

Dept. : CSE

Third Internal Assessment Test Attendance Details

Sl. No	STUDENT NAME	DATE >	11/03/24		12/03/24		13/03/24		Signature of the student
		TIME >	10.00 am 11.30 am	02.00 pm 03.30 pm	10.00 am 11.30 am	02.00 pm 03.30 pm	10.00am 11.30am	02.00 pm 03.30 pm	
		SUBJECTS >	ATC (21CS81)	CN (21CS82)	DBMS (21CS83)	AI (21AI84)	BMI (21BM186)	CIV (21CIV87)	
		USN							
1	VANDANA H	1MJ21CS111	P	P	P	P	P	P	
2	VEDAMURTHA G M	1MJ21CS112	P	P	P	P	P	P	
3	VEENA Y H	1MJ21CS113							
4	VENKATESH K	1MJ21CS114	P	P	P	P	P	P	
5	VENKATESH	1MJ21CS115	P	P	P	P	P	P	
6	VINAY	1MJ21CS116	P	P	P	P	P	P	
7	VISHAL JAGADISH	1MJ21CS117	P	P	P	P	P	P	
8	VISHAL KUMAR	1MJ21CS118	P	P	P	P	P	P	
9	VISHALKUMAR	1MJ21CS119	P	P	P	P	P	P	
10	YASHASWINI C	1MJ21CS120	P	P	P	P	P	P	
11	YUKTHI H	1MJ21CS121	P	P	P	P	P	P	
12	ARUN KUMAR	1MJ21CS400	P	P	P	P	P	P	
13	HARSHAVA J	1MJ21CS401	P	P	P	P	P	P	
14	GOKUL G.S.	1MJ21CS402	P	P	P	P	P	P	
15	PARVATHI K. V	1MJ21CS403	P	P	P	P	P	P	
16	PUNITH K.R.	1MJ21CS404	P	P	P	P	P	P	
TOTAL No. OF STUDENTS PRESENT :									
TOTAL No. OF STUDENTS ABSENT :									
ROOM SUPERINTENDENT NAME & SIGNATURE WITH DATE :									
ESN# (Candidates Not Malpractice)									
SQUAD SIGNATURES									

Verified By : Mrs. Jyoti Patnaik
Designation : Test Coordinator
Signature with date : 13/3/24

Approved By : Dr. Mahesh G.H.
Designation : HOD
Signature with date :

	MS ENGINEERING COLLEGE BANGALORE	Form No.: R/ PP-02/ 13/ 03
	Title: Internal Examination Time Table	

Department : ECE

Semester : VIII

Date : 2/05/2023

Test No : 1) 3

Date	SEM	SUBJECT CODE AND TIMINGS
		9.30 AM to 11.00AM
		Subject Name and Code
5/05/2023	8	Wireless and Cellular Communication (18EC81)
6/05/2023	8	Network Security (18EC821)

Prepared by : Tejaswini C Designation : Professor Signature :	Approved by : Sunitha P. H Designation : HOD and Professor Signature :

	M S ENGINEERING COLLEGE BANGALORE Title: Internal Examination Time Table	Form No.: R/ PP-02/ 13/ 01

Department : ECE **Date : 19/5/2023**

Semester : VI **Test No : 2**

Date	Time	
	9:30 AM to 10:45 AM	2:00PM to 3:15 PM
	Subject Name and Code	
25/5/2023	Digital Communication (18Ec61)	Embedded Systems (18EC62)
26/5/2023	Microwave and Antennas (18EC63)	Digital system Design using Verilog (18EC644)
27/5/2023	Programming in Java (18CS653)	

Prepared by : Savitha S C Designation :Asst.Professor Signature :	Approved by :Dr.Sunitha P H Designation : HOD and Professor Signature :

	M S ENGINEERING COLLEGE BANGALORE Title: Internal Examination Time Table	Form No.: R/ PP-02/ 13/ 01

Department : ECE

Semester : VI

Date : 28/6/2023

Test No : 3

Date	Time	
	9:30 AM to 10:45 AM	2:00PM to 3:15 PM
	Subject Name and Code	
03/7/2023	Digital Communication (18EC61)	Embedded Systems (18EC62)
04/7/2023	Microwave and Antennas (18EC63)	Digital system Design using Verilog (18EC644)
05/7/2023	Programming in Java (18CS653)	

Prepared by : Savitha S C	Approved by :Dr.Sunitha P H
Designation :Asst.Professor	Designation : HOD and Professor
Signature :	Signature :

	M S ENGINEERING COLLEGE BANGALORE Title: Internal Examination Time Table	Form No.: R/ PP-02/ 13/ 01

Department : Electronics and communication

Date : 19-02-2024

Semester : III and V

Test No : II

Date	Time	
	9:30 AM to 10:45 AM	2:00PM to 3:15 PM
	Subject Name and Code	
27-02-2024	Mathematics(22MAT31) Digital Communication(21EC51)	Digital System Design using Verilog(BEC302) Computer organization and ARM Microcontroller(21EC52)
28-02-2024	Electronic Principles and Circuits (BEC303) Computer Communication Networks(21EC53)	Network Analysis(BE304) Electro magnetic waves(21EC54)
29-02-2024	Computer Organization and Architecture(BEC306C) Research methodology(21EC56)	IoT for Smart Infrastructure (BEC356D)

Prepared by : Dr. Kiran B	Approved by : Dr. Sunitha P H
Designation : Assoc Prof	Designation : Prof and HOD
Signature : 19.2.24	Signature : PHC

	M S ENGINEERING COLLEGE BANGALORE	Form No.: R/ PP-02/ 13/ 01
	Title: Internal Examination Time Table	

Department : ECE

Semester : VIII

Date : 11/03/2024

Test No : 1

Date	Time
	9:30 AM to 10:30 AM
	Subject Name and Code
14/03/2024	Wireless and Cellular Communication – 18EC81
15/03/2024	Network Security – 18EC821

Prepared by : Dr. Kiran B Designation : Associate Professor Signature :	Approved by : Dr. Sunitha P H Designation : Professor and HoD Signature :

	M S ENGINEERING COLLEGE BANGALORE	Form No.: R/ PP-02/ 13/ 01
	Title: Internal Examination Time Table	

Department : ECE

Semester : VIII

Date : 02/05/2024

Test No : III

Date	Time
	9:30 AM to 10:30 AM
	Subject Name and Code
08/05/2024	Wireless and Cellular Communication – 18EC81
09/05/2024	Network Security – 18EC821

Prepared by : Dr. Kiran B	Approved by : Dr. Savitha P H
Designation : Associate Professor	Designation : Professor and HoD
Signature :	Signature :

LESSON PLAN

Subject: CAED Subject Code: BCEDK203

Branch: ISE Semester: II D

Lesson No.	Module No.	Planned Date	Topic	Remarks
1		14/3/24	Introduction to CAED and CO, PO, PSO, PEO, Vision & Mission	
2	1	18/3/24	Orthogonal projection: HP VP PP Projection of points, problems	
3	1	21/3/24	projection of lines: True length and True angle - problems	
4	1	25/3/24	Apparent length and angles problems	
5	1	28/3/24	projection of planes: Triangle Square Lamina - problems	
6	1	30/3/24	Rectangle and pentagonal Lamina - problems	
7	1	01/4/24	Hexagonal Lamina problems	
8	1	04/4/24	Circular Lamina - problems	
9	2	15/4/24	projection of Solids: Square Pyramid and Tetrahedron	
10	2	18/4/24	pentagonal and hexagonal pyramids	
11	2	25/4/24	Cube, Square prism	
12	2	29/4/24	Cone	
13	2	02/5/24	pentagonal prisms	
14	2	6/5/24	Hexagonal prisms	
15	3	09/5/24	Isometric projection: planes Pyramid, Stab, Cube, Sphere	

Signature of Faculty HOD

WORK DONE STATEMENT

Subject: CAED

Lesson No.	Module No.	Actual Date of completion	Topic Covered	Remarks
1			Introduction to CAED. Contents CO, PO, PSO, PEO, Vision & Mission	
2	1	18/3/24	Orthogonal projection, HP, VP, PP projection of points, problems	
3	1	21/3/24	projection of points - problems projection of lines: Introduction	
4	1	28/3/24	projection of lines - True length and True Inclinations - problems	Class Suspended due to holi
5	1	30/3/24	Apparent length and angles - problems.	
6	1	02/4/24	projection of planes: Triangular and Square lamina problems	
7	1	4/4/24	pentagon and Hexagonal Lamina problems	
8	1	15/4/24	Circular lamina and Sq. lamina & angle problems	
9	2	18/4/24	projection of Solids: Square pyramid resting edge + Slant edge on HP	
10	2	19/4/24	Hexagonal pyramid: Slant Surface on HP + axis inclined with VP	
11	2	29/4/24	Hexagonal prism - & angle Square prism - edge	
12	2	02/5/24	pentagonal prism Tutorial hour	
13	2	09/5/24	Cone with axis inclined, generator on HP + Cube	
14	3	13/5/24	Isometric projection: Planes, pyramid, Slab, Cube, Sphere, Cone, hemisphere	
15	3	16/5/24	Cylinder, Lamp hole frustum of Cone, Slab	

Signature of the Faculty

HOD

Principal

M S ENGINEERING COLLEGE
BANGALORE

Title: Calendar of Events First Year

Form No.: [illegible]

Academic Calendar for Even Semester of 2022-23 (MAY 2023-AUG 2023) Course: B.E (II SEM)

I	Month	Mon	Tue	Wed	Thu	Fri	Sat	No of Working Days		Events
								n	Cu	
1	MAY/JUN				25 COS	26	27	3	3	25th May- Commencement of Sem 14th -Annual Sports day 15th- Ethnic Day 16th – Nakshatra 21st- International Yoga Day 29th-Rakrid A1Assignment-I
2		29	30	31	1	2	3 SO	5	8	
3		5	6	7	8	9	10	6	14	
4		12	13	14	15	16	17 SO	5	19	
5		19	20	21	22	23	24	6	25	
6		26	27 A1	28	29 GH	30		4	29	
7	JULY						1 SO	4	29	T1- I IA Q1-Quiz-I A2- Assignment-2
8		3 ISO	4 FF	5 MAR	6	7	8 QI	6	35	
9		10 T1	11 T1	12 T1	13 T1	14	15 SO	5	40	
10		17 A2	18 PRS	19	20	21	22 PTM	6	46	
11		24	25	26	27	28	29 SO	5	51	
12		31						1	52	
13	AUG		1	2	3	4 MAR	5 SO	4	56	15th -Independence Day Q2-Quiz-2 T2-II IA
14		7 GH	8	9	10	11	12 T2	6	62	
15		14 T2	15 GH	16 T2	17 T2	18	19 SO	4	66	
16		21 PRS	22	23 FF	24 ISO	25	26	6	72	
17		28	29	30	31			4	76	
18	SEP					1	2 SO	1	77	T3- III IA
19		4 T3	5 T3	6 T3	7	8 MAR	9 LWD	6	83	
	TOTAL	15	14	15	15	16	08	83		

EVENTS

MAR: Monthly Attendance Report	ISO: File	[illegible]	CRM: Class Representative Meeting
GH: Government Holiday	[illegible]	FM: Faculty Meeting	PTM: Parents Teachers Meeting
PRS: Progress Report Submission	CTA1: Class Teachers [illegible]	[illegible]	[illegible] Feedback by Students

Prepared By: [illegible]
Designation: Asst Professor
Sign:

Verified By: Dr. [illegible]
Designation: HOD/Dean/ Vice Principal
Sign:

Approved By: [illegible]
Designation: Principal
Sign:

M.S. Engineering College
Navarathna Agraham,
[illegible]

M S ENGINEERING COLLEGE BANGALORE	Form No.: R/ PP-02/20/ 01
Title: Calendar of Events	

Academic Calendar for Odd Semester (SEPT 2023-JAN 2024) Course: B.E (I SEM)

Week No	Month	Mon	Tue	Wed	Thu	Fri	Sat	No of Working Days W	Cum	Events
1	SEPT	4 COS	5	6	7	8	9	6	6	COS: Commencement of Semester 4th – 14th – Induction Programme
2		11	12	13	14	15	16 SO	5	11	
3		18 GH	19	20	21	22	23	5	16	
4		25	26	27	28	29	30 SO	4	20	
5	OCT	2 GH	3	4	5	6	7 SO	4	24	2nd -Gandhi Jayanthi 15th -24th -Navratri Color week 23rd Ayudha pooja 24th -Vijaya Dashami A1- Assignment-I
6		9	10	11	12	13	14	6	30	
7		16	17	18	19	20	21 SO	5	35	
8		23 GH	24 GH	25	26	27	28	4	39	
9		30 A1	31 MAR					2	41	
10	NOV			1 GH	2 T1	3 T1	4 SO	2	43	1st - Kannada Rajyotsava T1- I IA Test 14th -Deepavali 11th – Code Challenge 25th – Group Discussion A2- Assignment 2
11		6 T1	7 T1	8	9	10	11	6	49	
12		13	14 GH	15	16	17 CRM	18 SO	4	53	
13		20 PTM	21	22	23	24	25	6	59	
14		27	28	29 A2	30			3	62	
15	DEC					1 T2	2 SO	1	63	T2- II IA Test 25th – Christmas 9th Miss Match Day A3- Assignment 3
16		4 T2	5 T2	6 T2	7 MAR	8	9	6	69	
17		11	12	13	14	15 PRS	16 SO	5	74	
18		18 PTM	19	20	21	22	23	6	80	
19		25 GH	26	27	28 [illegible]	29 A3	30 SO	4	84	
20	JAN	1 MAR	2 T3	3 T3	4 T3	5 T3	6 LWD	6	90	T3- III IA Test LWD-Last Working Day
	TOTAL	16	18	17	18	19	[illegible]	90		

FF: Faculty Feedback by Students	SO : File	CRM: Class Representative Meeting
PRS : Progress Report Submission	MAR: Monthly Attendance Report	CTM : Class Teachers Meeting
GH: Government Holiday	SO: Saturday Off	PTM : Parents Teachers Meeting

Prepared By: Mrs.Sushma	Verified By: Dr.Ravikumar H R	Approved By: Dr.P.Mahadevaswamy
Designation: Asst.Professor	Designation: First Year Co-Ordinator	Designation: Principal
Signature:	Signature:	Signature:

Principal
M.S. Engineering College
Navarathna Agrahara, Sadahalli Post,
Bangalore-562 110

M S ENGINEERING COLLEGE, BENGALURU

(Affiliated to Visvesvaraya Technological University, Belagavi & Approved by AICTE, New Delhi)
(Accredited by NAAC, UGC 2(f) Status and An ISO 9001-2015 Certified Institution)
Navarathna Agrahara, Sadahalli post, Off International Airport Road (NH7), Bengaluru-562110

DEPARTMENT OF APPLIED SCIENCES

Calendar of Events

Academic Calendar for EVEN Semester [redacted] 2024-JUNE [redacted] Course: B.E [redacted]

Week No	Month	Mon	Tue	Wed	Thu	Fri	Sat	No of Working Days		Events
								N	Cum	
1	MAR			4 COS	7	8 [redacted]	9	3	3	COS: Commencement of Semester 6th-16th - Induction Programme 8th – Maha shivaratri 29th- Good Friday 14th – Fresher's Talent's Day 30th-Linking Holiday
2		11	12	13	14	15	16 SO	5	8	
3		18	19	20	21	22	23	6	14	
4		25	26	27	28	29 GH	[redacted]	5	19	
5	APR	1	2	3	4	5	6 [redacted]	5	24	9th- Ugadi T1- II IA Test(19th to 24th) A1- Assignment-1 25th- Technical Talk By Expert
6		8	9 GH	10	11	12	13	5	29	
7		15	16	17 A1	18 MAR	19 [redacted]	20 [redacted]	5	34	
8		22 [redacted]	23 [redacted]	24 [redacted]	25	26 FF	27 PTM	6	40	
9		29	30					2	42	
10	MAY			1 GH	2	3	4 [redacted]	3	44	1st- Labour Day T2 -II IA Test(17th to 22nd) A2 Assignment-2
11		6 PRS	7	8	9	10	11	6	50	
12		13	14	15	16 A2- MAR	17 T2	18 SO	5	55	
13		20 T2	21 T2	22 T2	23	24	25 ISO	6	61	
14		27	28	29	30	31 PRS		5	66	
15	JUN						1 SO	0	66	
16		3	4	5	6	7	8 PTM	6	72	T3-III IA Test(24th to 27th) LWD-Last Working Day
17		10	11	12	13	14 FF	15 SO	5	77	
18		17	18	19	20	21	22	6	83	
19		24 T3	25 T3	26 T3	27 T3	28 MAR	29 LWD	6	89	
	TOTAL	16	15	16	17	15	10	89		

FF: Faculty Feedback by Students	ISO : File , SO: Saturday Off	PTM : Parents Teachers Meeting
PRS : Progress Report Submission	MAR: Monthly Attendance Report	GH: Goverament Holiday

Prepared By: Mrs. Sushma Designation: [redacted] Professor Signature:	Verified By: Dr. Ravikumar H R Designation: First Year Co-Ordinator Signature:	Approved By: Dr.P. [redacted] Designation: Principal Signature:

M.S. Engineering College
Navarathna Agrahara, Sadahalli Post,
Bangalore-562 110

MS ENGINEERING COLLEGE

Affiliated to Visvesvaraya Technological University, Belagavi, Approved by AICTE, New Delhi,
Accredited by NAAC, UGC 2(f) Status and (An ISO 9001-2015 Certified Institution

Off. Bengaluru International Airport Road, Navarathna Agrahara,
Sadahalli Post, Bengaluru - 562 110.
Website : www.msec.ac.in

Name of the Staff Member	Dr. R. Mahadeeraswamy
Academic Year	2023-24
Semester Commencement Date	06/03/2024
Semester Closing Date	
Class & Branch	II E EC + AIML
Subject Code	BCEDX203
Subject Name	C.A-ED

Reviewer	REVIEWS at the End of the			End of Semester (Last Working day)
	1st Month Date.. 06/3/24	2nd Month Date. 30/4/24	3rd Month Date... 31/5/24	
Staff				
HOD				
Principal				

ATTENDANCE

Class : 7 E | EC A3 Subject with Code : BCAED, BCEDL2

Sl. No.	USN	NAME	Day	19	19	20	20	25	26	27	27
			Month	3	3	3	3	3	3	3	3
	1ME23			1	2	3	4	5	6	7	8
1	EC 001	Adarsha AB		1	2	3	4	4	4	4	5
2	002	Akhilesh GM		1	2	3	4	5	6	7	8
3	003	Anoorya Talavar MN		1	2	3	4	5	6	7	8
4	004	Archana CM		1	2	3	4	5	6	7	8
5	005	Bharath KM		1	2	3	4	5	6	6	7
6	006	Gorla Naren		1	2	3	4	4	4	4	5
7	007	Harshitha SK		1	2	3	4	5	6	7	8
8	008	Mythri HN		1	2	3	4	5	6	7	8
9	009	Nikhil Kumar GS		1	2	3	4	4	4	5	6
10	010	Nithin Kumar SR		1	2	3	4	4	4	4	5
11	011	Pujeeth G		1	2	3	4	5	6	7	8
12	012	Rahul Kumar K				1	2	3	4	5	6
13	013	Ranjith PD				1	2	3	4	5	6
14	014	Rishitha G		1	2	3	4	5	6	7	8
15	015	Sanjay MC		1	2	3	4	4	4	4	5
16	016	Sahith Subbappa Biradar		1	2	3	4	5	6	7	8
17	017	Sharanabasava V Hadapad		1	2	3	4	5	6	7	8
18	018	Shirisha		1	2	3	4	5	6	7	8
19	019	Shreyas MG		1	2	3	4	5	6	6	7
20	020	Shreyas V						1	2	3	4
21	021	Sujatha		1	2	3	4	5	6	7	8
22	022	Sumanth CS		1	2	3	4	5	6	7	8
23	AI 001	Abdur Rahaman Khan				1	2	3	4	5	
24	002	Abhishek K Rathod						1	2	3	4
25	003	Ambika		1	2	3	4	5	6	7	8
	No. of Abs.										
	Initials										

IENT

12/3	26/4	3/4	3/4	3/4	16/4	16/4	17/4	17/4	19/4	22/4	23/4	Percentage	IA1	IA2	IA3		Average Assignment Marks	Final CIE Marks	SEE Marks	Total (CIE + SEE)	Result
9	10	11	12	13	14	15	16	17	18	19	20										
6	7	8	9	10	11	12	13	14	15	16	17	[illegible]						31	33	64	P
9	10	11	12	13	14	15	16	17	18	19	20	[illegible]						20	29	49	P
9	10	11	12	13	14	15	16	17	18	19	20	[illegible]						22	20	42	P
9	10	11	12	13	14	15	16	17	18	19	20	[illegible]						46	41	87	P
8	9	10	11	12	13	14	15	16	17	18	19	[illegible]						20	20	40	P
6	7	8	9	10	11	12	13	14	15	16	17	[illegible]						30	40	70	P
9	10	11	12	13	14	15	16	17	18	19	20	[illegible]						35	35	70	P
9	10	11	12	13	14	15	15	15	16	17	18	[illegible]						28	42	70	P
7	7	7	8	9	10	11	12	13	14	15	16	[illegible]						34	26	60	P
6	7	8	9	10	11	12	13	14	15	16	17	56						23	07	30	F
7	9	9	10	11	12	13	14	15	16	17	18	56						23	44	67	P
7	8	9	10	11	12	13	13	13	14	15	16	56						22	29	51	P
7	8	9	9	9	10	11	12	13	14	15	16	56						28	28	56	P
9	10	11	12	13	14	15	16	17	18	19	20	70						48	44	92	P
6	7	8	9	10	11	12	13	14	15	16	17	[illegible]						39	45	84	P
9	10	11	12	13	14	15	16	17	18	19	20	[illegible]						33	36	69	P
9	10	11	12	13	14	15	16	17	18	19	20	[illegible]						40	43	83	P
9	10	11	12	13	14	15	16	17	18	19	20	[illegible]						47	45	92	P
8	9	10	11	12	13	14	15	16	17	18	19	[illegible]						40	42	82	P
5	6	7	8	9	10	11	12	13	14	14	15	[illegible]						20	21	41	P
9	10	11	12	13	14	15	16	17	18	19	20	[illegible]						42	43	85	P
9	10	11	12	13	14	15	15	15	16	17	18	[illegible]						21	30	51	P
7	7	7	8	9	10	11	12	13	14	15	16	[illegible]						35	22	57	P
5	6	7	8	9	10	11	12	13	14	15	16	[illegible]						32	31	63	P
9	10	11	12	13	14	15	16	17	18	19	20	[illegible]						38	20	58	P
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]						[illegible]	[illegible]	[illegible]	[illegible]

MS ENGINEERING COLLEGE

Off. Bengaluru International Airport Road, Navarathna Agrahara, Sadahalli Post, Bengaluru - 562 110.

PERSONAL TIME TABLE

Academic year 2023-24 Semester (ODD/EVEN) EVEN

NAME OF THE FACULTY Dr. [illegible] WITH EFFECT FROM 26/3/2024

TIME	1	2	3	4	5	6	7
MONDAY						CAED III D (ISE)	
TUESDAY		CAED III E (ECE)					
WEDNESDAY						CAED III E (ECE)	
THURSDAY		CAED III D (ISE)					
FRIDAY							
SATURDAY							

Signature of the Faculty

HOD

Principal

	M S ENGINEERING COLLEGE BANGALORE Title: Time Table	Form No.: R/ PP-02/ 02/ 01

Department: Engg.Chemistry	Branch: CSE	Sec: A	Effective Date : 05.05.2025
Semester: II	Class Teacher : Prof. PRAKASH A M		Room No : 310

DAY/TIME/ PERIOD	09:00-9:50	9:50-10:40	10:40-03:30	11.30-11.45	11:45-12:40	12:40- 01:35	01:35-02:30	02:30-03:25	03:25- 04:20
	1	2	3		4	5		6	7
MON	ENG	JAVA	CHE	TEA BREAK	CED A1/ CHE A2 / MAT A3		LUNCH BREAK	MAT	IE
TUE	CHE A1/ JAVA A2 / CED A3		MAT		IE	CHE		CED	CED
WED	MATA1/ CED A2 / JAVA A3		ENG		JAVA	SFH		MAT	MENTORING
THU	IE	SFH	JAVA		CHE	KAN		JAVA A1/ MATA2 / CHEA3	
FRI	IE	CHE	MAT		MAT	JAVA		CED	CED
SAT	JAVA	IE	CHE		MAT	KAN		LIB/TUTORIAL / SPORTS	

SUB CODE	NAME OF THE SUBJECT	FACULTY IN CHARGE	TOTAL NO OF PERIODS ALLOTTED
BMATS201	Mathematics-II forCSE Stream	Ms.BHAVYASHREE.S	6
BCHES202	Applied Chemistry for CSE Stream	DR RAVIKUMAR H R	5
BCEDK203	Computer-Aided Engineering Drawing	Mr PRAKASH A M	4
BESCK204C	Introduction to Electronics Communication	Dr. KIRAN	5
BPLCK205C	Basics of JAVA programming	Mrs.CHAITHRA	5
BPWSK206	Professional Writing Skills in English	Mr.AVINISH	2
BKSKK207/BKBKK207	Samskrutika Kannada/ Balake Kannada	Mr.MURALIKRUSHNA/Prof.PASHA	2
BSFHK258	Scientific Foundations of Health	Mrs.PREETHI R	2

Prepared By: Mrs. SUSHMA Designation: Asst.Prof Sign:	Verified By: Dr RAVIKUMAR H R Designation: HOD & First year coordinator Sign:	Approved By: Dr.P.MAHADEVASWAMY Designation: Principal Sign:

Principal
M.S. Engineering College
Navarathna Agrahara, Sadahalli Post
Bangalore-562 110

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Form No.: R/PP-02/05/01

DEPARTMENT OF BASIC SCIENCE

Time Table for the Academic Year 2023-24 (Even semester) WEF : 06/03/2024

Cycle: Physics Cycle		Sem & Branch: II CSE		Sec: A		Class Teacher: Bhavyashree S			Room No : 116
[illegible]	[illegible]	9:50-10:40	[illegible]	[illegible]	11:45-12:40	[illegible]	01:35-02:30	02:30-03:25	03:25- 04:20
	1	2	3		4	5		6	7
MON	PHY	POP	ENG		MAT	IDT		PHY A1/ POP A2/ MAT A3	
TUE	MAT	IOT	KAN		ME	POP		PHY	LIB
WED	POP	ME	ENG		PHY	MAT		IOT	SPORTS
THU	IOT	ME	MAT		POP A1/ MAT A2/PHY A3			POP	KAN
FRI	MAT A1/PHY A2/ POP A3		PHY		IDT	ME		IOT	TUTORIAL
SAT	MAT	PHY	POP		IOT	ME		SPORTS	

Sl No	SUB CODE	NAME OF THE SUBJECT	FACULTY IN CHARGE	TOTAL NO OF PERIODS ALLOTTED
1	BMATS201	Mathematics-II for CSE Stream	Ms Bhavyashree. S	4
2	BPHYS202	Applied Physics for CSE stream	Ms Preethi R / Mrs. keerthi S	4
3	BPOPS205	Principles of Programming using C	Mr P. Rajan	4
4	BESCK204D	Introduction to Mechanical Engineering	Mr Mohan kumar	4
5	BETCK205H	Introduction to internet of Things(IOT)	Mrs Savitha	4
6	BENGK206	Professional Writing Skills in English	Mr Avinash	2
7	BKSK207/BKBK207	Samskrutika Kannada/ Balake Kannada	Mr Murali Krishna / Mrs KeerLai S	2
8	BIDTK258	Innovation and Design Thinking	Dr Shantha kumar	2

Prepared By: Mr SHARATH K C	Verified By: Dr RAVIKUMAR H R	Approved By: Dr. P. MAHADEVASWAMY
Designation: Assistant professor	Designation: HOD & First year coordinator	Designation : Principal
Sign:	Sign:	Sign:

Principal
M.S. Engineering College
Navarathna Agrahara, Sadahalli Post,
Bangalore-562 110

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Form No.: R/PP-02/05/01

DEPARTMENT OF BASIC SCIENCE

Time Table for the Academic Year 2024-25 (Odd semester) WEF : 28/09/2024

Cycle: Engg. Chemistry | Sem & Branch: I CSE | Sec: A | Class Teacher: Mrs. RADHA | Room No: 104

DAY/TIME / PERIOD	09:00-9:55	9:55-10:50	10:50-11:45	11.45-12.00	12:00-12:50	12:50-01:40	01:40-02:30	02:30-03:30	03:30-04:20
	1	2	3		4	5		6	7
MON	CAED		PYT	TEA BREAK	CHE A1/ CAED A2/PYT A3		LUNCH BREAK	CIV	MENTOR
TUE	PYT A1/ MAT A2/CHE A3		CHE		CIV	SFH		ENG	MAT
WED	IC	MAT	CIV		PYT	CHE		MAT A1/PYT A2 / CAED A3	
THU	MAT	PYT	CHE		CAED A1 /CHE A2 /MAT A3			CAED	
FRI	CIV	CHE	MAT		CAED			PYT	LIBRARY
SAT	REMEDIAL CLASS				REMEDIAL CLASS			REMEDIAL CLASS	

Sl. No	SUB CODE	NAME OF THE SUBJECT	FACULTY IN CHARGE	TOTAL NO OF PERIODS ALLOTTED	
				THEORY	PRACTICAL
1	BMATS101	Mathematics-I for CSE Stream	Mrs. RADHA	4	6
2	BCHES102	Applied Chemistry for CSE Stream	Dr RAVIKUMAR H R	4	6
3	BCEDK103	Computer-Aided Engineering Drawing	Mr. RAJANIKESH M K	6	6
4	BCEDK104A	Introduction to Civil Engineering	Mrs. SWETHA K S	4	
5	BPLCK105B	Introduction to Python Programming	Dr KIRAN	4	6
6	BENGK106	Communicative English	Mr. SHIVANANDA	1	
7	BCIVK107	Indian Constitution	Mrs. KEERTHI	1	
8	BSFHK158	Scientific Foundations of Health	Ms. R PREETHI	1	

Prepared By: Mr SHARATH K C
Designation: Assistant professor
Sign:

Verified By: Dr RAVIKUMAR H R
Designation: HOD & First year coordinator
Sign:

Approved By: Dr. N RANAPRATHAP REDDY
Designation: Principal
Sign:

	M S ENGINEERING COLLEGE BANGALORE Title: Time Table	Form No.: [illegible]

Cycle: Engg.Chemistry	Branch: CSE	Sec: A	Effective Date: [illegible]
Semester: I	Class Teacher: [illegible]		Room No: 16

DAY/TIME / PERIOD	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]-04:30
	1	2	3		4	5		6	7
MON	ENG	PYTHON	CHE	TEA BREAK	CAED A1/ CHE A2/ MAT A3		LUNCH BREAK	MAT	TUTORIAL
TUE	CHE A1/ MAT A2/ PYTHON A3		MAT		CIVIL	CHE		CAED	
WED	PYTHON A1/ CAED A2/ CHE A3		ENG		PYTHON	SFH		TUTORIAL	IC
THU	CIVIL	IC	CHE		MAT	TUTORIAL		MAT A1/ PYTHON A2/ CAED A3	
FRI	MAT	CIVIL	CHE		TUTORIAL	PYTHON		CAED	
SAT	PYTHON	SFH	MAT		CHE	MENTOR		TUTORIAL	

SUB CODE	NAME OF THE SUBJECT	FACULTY IN CHARGE	TOTAL NO OF PERIODS ALLOTTED
BMATS101	Mathematics-I for CSE Stream	[illegible]	5
BCHES102	Applied Chemistry for CSE Stream	Dr RAVIKUMAR H R	5
BCEDK103	Computer-Aided Engineering Drawing	Mr RAJNEESH M. K	4
BESCK104A	Introduction to Civil Engineering	Mrs CHAITHANYA M B	3
BPLCK105B	Introduction to Python Programming	Ms P SUSHMITHA SINGH	4
BENGK106	Communicative English	Mr AVINASH	2
BICOK107	Indian Constitution	Prof PASHA	2
BSFHK158	Scientific Foundations of Health	Mrs CHAITHANYA M B	2

Prepared By: SHARATH K C	Verified By: Dr RAVIKUMAR H R	Approved By: Dr.P.MAHADEVASWAMY
Designation: Assistant professor	Designation: HOD & First year coordinator	Designation: Principal
Sign:	Sign:	Sign:

Principal
M.S. Engineering College
Navarathna Agrahara, Sadahalli Post,
Bangalore-562 110

	M.S. ENGINEERING COLLEGE, BENGALURU Title: Question Paper	Form No.: R/ PP-02/ 15/01

USN

Department of Electronics & Communication Engineering

Internal Assessment Test – III

Academic Year 2023-24 (EVEN Sem: II Semester)
Section B & C

Subject: Introduction to Internet Of Things (IOT) | **Date: 29-06-2024**
Subject Code: BETCK205H | **Time: 2 PM to 3 PM**
Max. Marks: 25 | **Duration: 1 hr**

Note: Answer any two full questions, selecting one question from each part

PART A

Sl. No.		Questions	Blooms Taxonomy	CO	Marks Allotted
1	a.	With neat diagram, explain in detail about the components of vehicular IOT	L2	CO5	7
	b.	With necessary diagram, discuss in detail about Crime assistance in a smart IoT transportation system	L2	CO5	8
		OR			
2	a	With neat diagram, explain in detail about AmbuSens system, also explain the hardware used in the architecture	L2	CO5	7
	b.	Discuss in detail about the advantages of health care IOT	L2	CO5	8

PART B

Sl. No.		Questions	Blooms Taxonomy	CO	Marks Allotted
3	a.	Discus in detail about the components of healthcare IOT	L2	CO5	7
	b	Write a short note on Machine learning, also explain the advantages of machine learning	L2	CO5	8
4	a.	With necessary diagram, explain the architecture of vehicular IOT	L2	CO5	7
	b.	Discuss in detail about the types of machine learning, also mention the challenges in machine learning	L2	CO5	6

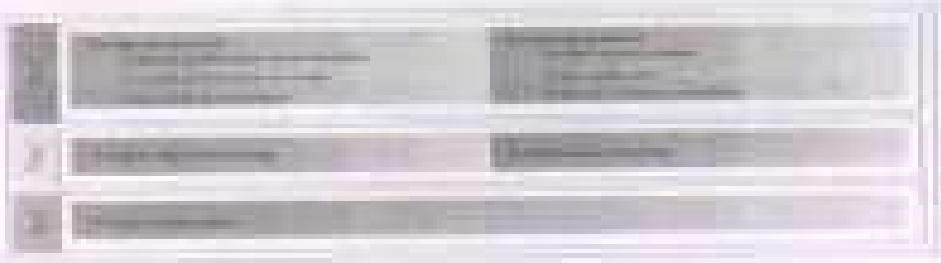
Prepared by: Anoob B Designation: Assistant Professor Signature:	Approved by: Dr. Smitha P H Designation: Professor and HOD Signature:

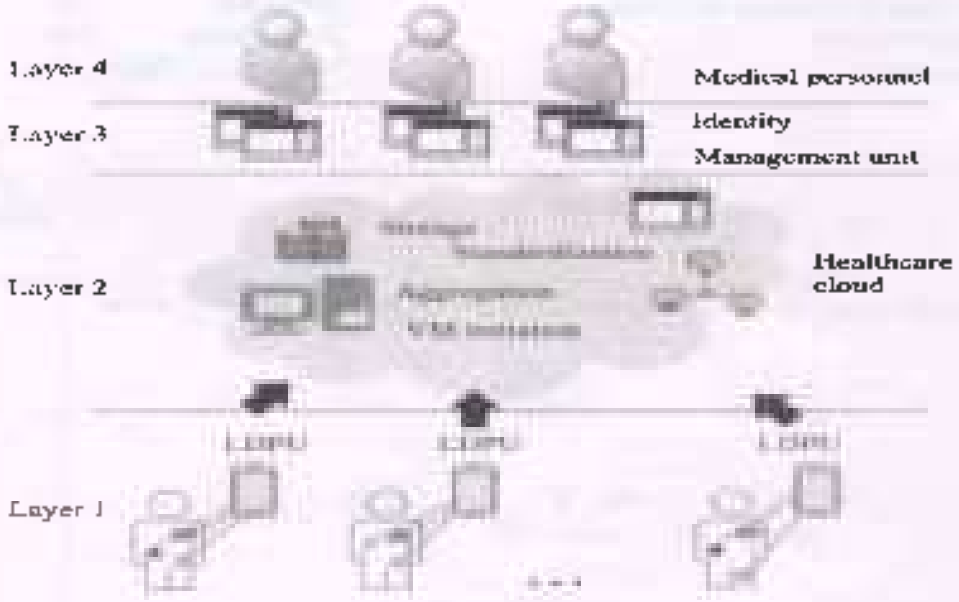
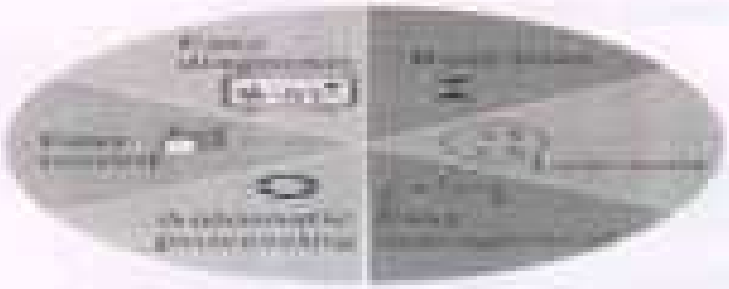
M S ENGINEERING COLLEGE, BANGALORE-562110

Title: Scheme of Solution for the III Internal Assessment Test Month and Year June 2024

Subject: Introduction to Internet Of Things
Subject Code: BETCK205H
Faculty Name: Anoob B

Semester : II
Total Marks : 25
Total No. Of Pages: 4

Q. No	Solution	Marks Distribution
1a	Components of Vehicular IOT: Diagram and Explanation 2 Marks, explanation 5 Marks  Figure 14.2 Components of vehicular IoT Sensors, Internal and External, Satellites- vehicle tracking, Wireless- communication Wi-Fi, Bluetooth, and GSM, RSU, Cloud and fog computing, analytics	7M
1b	Crime assistance: Architecture 2 Marks, Explanation: 3 Marks.  Figure 14.4 Architecture of Fog-FISVER Crime definition downloader, Crime definition storage, Algorithm launcher, Event dispatcher: This is another key component of Tier 1. The event dispatcher is responsible for accumulating the data sensed from vehicles and the image processor. Event notifier: It transfers the data to the fog-FISVER STS fog infrastructure, after receiving it from the attached sensor nodes in the vehicle. Data gatherer: This is an intermediate component between the event notifier and the physical sensor; it helps to gather sensed data. Virtual sensor interface: Multiple sensors that sense data from different locations of the vehicle are present in the system.	5M

Q. No	Solution	Marks Distribution
	Ambusen system: Architecture-2 Marks, Explanation 2 marks, Hardware: 3 Marks	
2a.		7M
	Figure 14.4 Layered architecture of AmbuSens	
	Hardware:) Optical Pulse Sensing Probe: It senses the photoplethysmogram (PPG) signal and transmits it to a GSR expansion module, ECG,EMG, Communication module, LDPU	
2b.		5M
	(a) Advantages of healthcare IoT	
	Real-time data monitoring: doctor to observe a patient's health condition in real-time even from a remote location, Low cost: Healthcare IoT systems facilitate users with different services at low cost, Easy management: Healthcare IoT is an infrastructure that brings all its end users under the same umbrella to provide healthcare services, Automatic processing: A healthcare unit consists of multiple subsystems, for which manual interventions are required, Easy record-keeping:, Easy diagnosis: We have already explained that a healthcare IoT system stores the data of the patient in a secure manner. Sometimes, for diagnosing a disease, a huge chunk of prior data is required.	

Q. No.	Solution	Marks Distribution
3a	Components of health care IOT Explanation: 7 Marks	

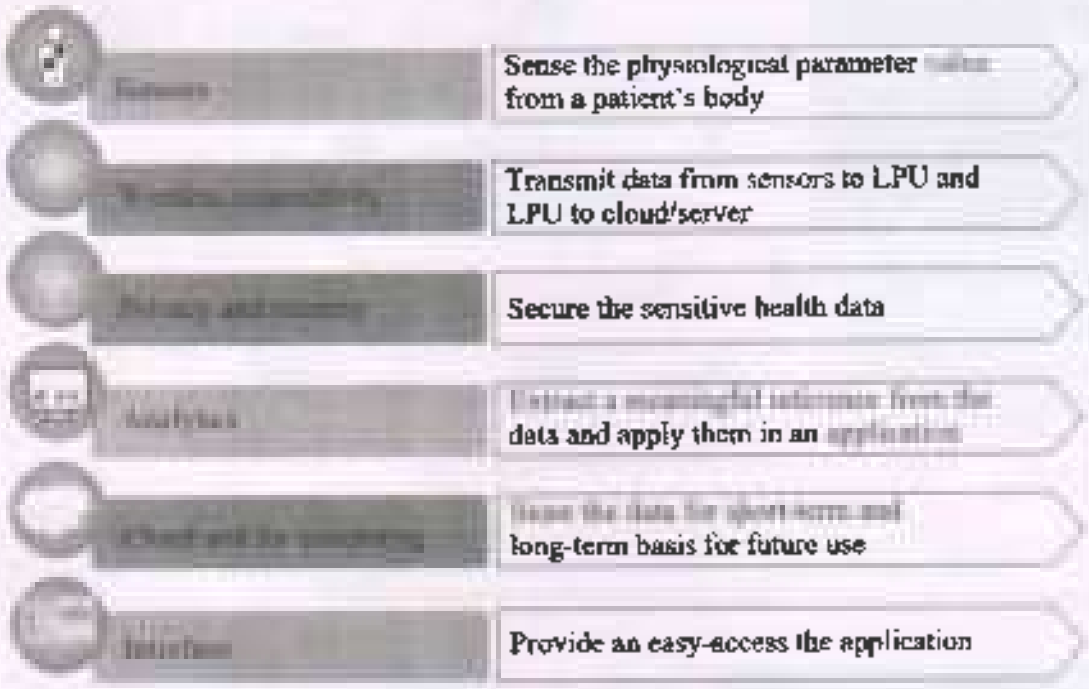


Figure 14.2 Components of healthcare IoT

3b. Machine learning 1mark, Advantages of ML 5 Marks

Figure 17.1 Advantages of ML

4a. Vehicular IOT: Architecture-3 marks, Explanation – 4 Marks

Device: The device layer is the bottom-most layer, which consists of the basic infrastructure of the scenario of the connected vehicle. This layer includes the vehicles and road side units (RSU). **Fog:** In vehicular IoT systems, fast decision making is pertinent to avoid accidents and traffic mismanagement. **Cloud:** Fog computing handles the data processing near the devices to take decisions instantaneously. processing of huge data, fog computing is not enough. Therefore, in such a situation, cloud computing is used.

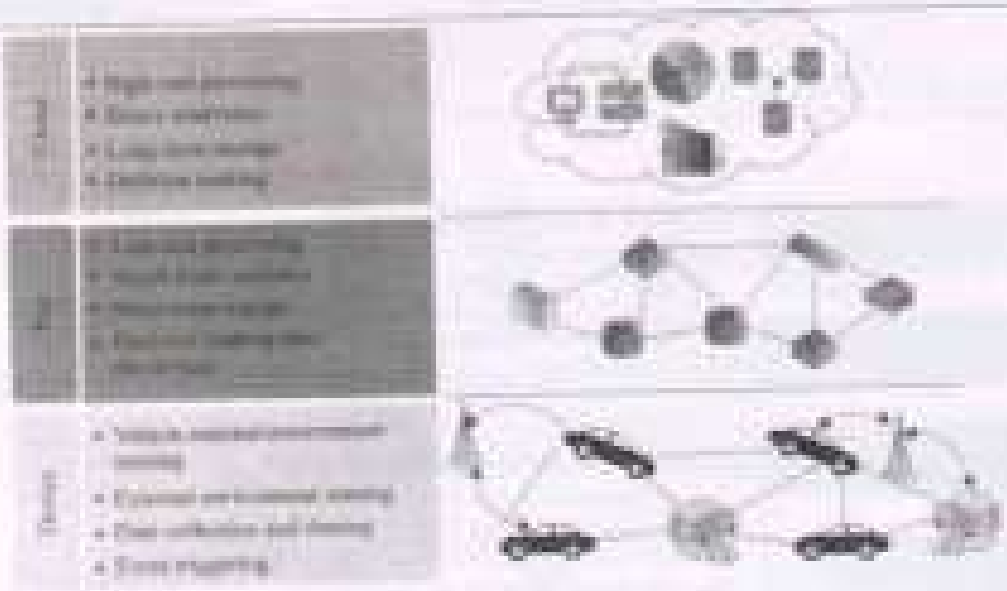


Figure 10.1 Architecture of vehicular IoT

Types of machine learning: 4 Marks, Challenges in machine learning: 2 Marks

Figure 10.2 Types of ML

(i) Data Description, (ii) Amount of Data, (iii) Erroneous Data, (iv) Selection of Model, (v) Quality of Model

Prepared by : Anoob B	Approved by : Dr. Sumitha P H
Designation : Assistant Professor	Designation : Professor and HOD
Signature :	Signature :

M S ENGINEERING COLLEGE

DEPARTMENT OF APPLIED SCIENCES

Title: 2nd IA Test Attendance & Room Superintendent's Report (SECTION : III)

Form No.:

R/ PP-02/ 17/ 01

Semester : II | BRANCH: ISE | LH-14

Sl. No.	USN	Name of the student	28.05.24 9.15AM-10.30AM BMATS201 Mathematics-II for CSE Stream	29.05.24 9.15AM-10.30AM BCHES202 Applied Chemistry for	27.05.24 9.15AM-10.30AM BESCK204A Introduction to Civil Engg	28.05.24 9.15AM-10.30AM BPLK205B Introduction to Python	29.05.24 9.15AM-10.30AM BENG206A Professional Writing Skills
1	1ME23I5001	RAJEEV RANJAN					
2	1ME23I5051	RAMYA S					
3	1ME23I5034	RETHVIK N					
4	1ME23I5036	S NARUL NANDAN					
5	1ME23I5037	SAKSHI					
6	1ME23I5038	SANVI G R					
7	1ME23I5039	SAURABH					
8	1ME23I5040	SAURABH KUMAR					
9	1ME23I5041	SHASHANK V S					
10	1ME23I5042	SHIVA KUMAR					
11	1ME23I5043	SHIVU R M					
12	1ME23I5044	SHRIHARSH A B S					
13	1ME23I5045	SHRUSTY V					
14	1ME23I5046	SHWETHA P					
15	1ME23I5047	SINCHANA SUBRAMANI					
16	1ME23I5048	SNIDHAR G					
17	1ME23I5049	SUDEEKSHA K C					

No of students present	16	16	16	14	17	
No of students absent	01	01	01	03	00	
No of students with MP	00	—	—	—		
Invigilators Sign						