ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
(ವಿ ಟಿ ಯು ಅಧಿನಿಯಮ ೧೯೯೪ ರ ಅಡಿಯಲ್ಲಿ ಕರ್ನಾಟಕ ಸರ್ಕಾರದಿಂದ ಸ್ಥಾಪಿತವಾದ ರಾಜ್ಯ ವಿಶ್ವವಿದ್ಯಾಲಯ)
VISVESVARAYA TECHNOLOGICAL UNIVERSITY
(State University of Government of Karnataka Established as per the VTU Act, 1994)
"JnanaSangama" Belagavi-590018, Karnataka, India

Prof. Dr. B. E. Rangaswamy, Ph.D.
REGISTRAR

Phone: (0831) 2498100
Fax : (0831) 2405467

REF: VTU/BGM/ACA/2023-24/ 3252

DATE: 30 SEP 2023

NOTIFICATION

Subject: Tentative Academic Calendar of 1st semester of B.Sc(Hons) program, 3rd and 5th semesters B.E./B.Tech. programs, 4th semester of MBA(IEV) program regarding...

Reference: Hon'ble Vice-Chancellor's approval dated: 30.09.2023

The tentative academic calendar concerned to 1st semester of B.Sc.(Hons) program, 3rd and 5th semesters B.E./B.Tech. programs, 4th semester of MBA(IEV) program for academic year 2023-24 are hereby notified as mentioned below;

	III semester B.E./B.Tech. (2022 scheme)	V semester B.E./ B.Tech. (2021 scheme)	I sem B.Sc(Hons)	IV semester MBA(IEV)*
Commencement of the Semester	25.10.2023	25.10.2023	03.10.2023	09.10.2023
Internship	----	25.10.2023 To 23.11.2023	---	----
Commencement of Classes	25.10.2023	25.11.2023	03.10.2023	09.10.2023
Last Working day of the Semester	10.02.2024	09.03.2024	25.01.2024	27.01.2024
Practical Examination/ Internship Viva Voce/ Project viva	12.02.2024 To 22.02.2024	11.03.2024 To 20.03.2024	29.01.2024 To 09.02.2024	01.02.2024 To 08.02.2024
Theory Examinations	26.02.2024 To 15.03.2024	22.03.2024 To 20.04.2024	12.02.2024 To 01.03.2024	
Commencement of NEXT Semester	18.03.2024	22.04.2024	04.03.2024	------

*Students have to complete skill certification and Internship within this duration (09.10.2023 to 27.01.2024)

Please Note:

- The academic sessions for semesters should commence on the **date mentioned** above.
- If required, the college can plan to have extra classes on 1st and 3rd Saturday and Sundays to complete academic activities within the academic duration mentioned.
- The faculty/staff shall be available to undertake any work assigned by the university.
- Notification regarding the Calendar of Events relating to the conduct of University **Examinations** will be issued by the Registrar (Evaluation) from time to time.
- Academic Calendar **may be modified** based on guidelines/directions issued in the future by UGC/AICTE/State Government.
- Academic Calendar is also applicable for **Autonomous Colleges.** If any changes are to be effected by Autonomous Colleges in the academic terms and examination schedule, they could do so with the approval of the University.
- If any suggestions/clarification/correction, please email to -**sbhvtuso@yahoo.com**

The Principals of Affiliated, Constituent and Autonomous Engineering Colleges, Chairpersons of the University departments are hereby informed to bring the academic calendar to the notice of all concerned.

Sd/-

REGISTRAR

To,

1. The Principals of all affiliated/ constituent /Autonomous Engineering Colleges under the ambit of VTU Belagavi.
2. The chairperson, of the Department of Mechanical Engineering /Civil Engineering /Computer Science and Engineering& Communication Electronics Engineering of the University.

Copy to.

1. To the Hon'ble Vice-Chancellor through the secretary to VC, VTU Belagavi for information
2. The Registrar (Evaluation), VTU Belagavi for information.
3. The Regional Directors (I/c) of all the regional offices of VTU for circulation.
4. The Director ITI SMU, VTU Belagavi for information and to make arrangements to upload Academic Calendar on the VTU web portal.
5. The Director of Physical Education, VTU Belagavi for information
6. The Director, Central Placement Cell, VTU Belagavi for information
7. The Special Officer Library, VTU Belagavi for information
8. All the concerned Special Officer/s and Caseworker/s of the academic section, VTU, Belagavi

30/05/23 BE

REGISTRAR

ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
(ಭಾರತ ಸಂವಿಧಾನದ 1994ನೇ ತಿದ್ದುಪಡಿ ಕಾಯಿದೆಯ ಪ್ರಕಾರ ಸರ್ಕಾರದಿಂದ ಸ್ಥಾಪಿತವಾದ ರಾಜ್ಯ ವಿಶ್ವವಿದ್ಯಾಲಯ)
VISVESVARAYA TECHNOLOGICAL UNIVERSITY
(State University of Government of Karnataka Established as per the VTU Act, 1994)
Phone : 0831-2498100 / 2405466
Fax : 0831-2405467
Email : registrar@vtu.ac.in
Web : https://vtu.ac.in

Ref. VTU/BOS/AC-PG-6th sem BE/2023-24/ 239 Dated: 15 APR 2024

NOTIFICATION

Subject: Tentative Academic Calendar of - IV semester MCA/M.Tech/M/Arch/M.Plan and VI semester B.E./B.Tech., programs academic calendar regarding...

Reference: 01. Dean faculty of Engineering approval dated 14.04.2024
02. The Hon'ble Vice-Chancellor's approval date: 15.04.2024

The tentative Academic Calendar of - IV semester MCA/M.Tech/M/Arch/M.Plan and VI semester B.E./B.Tech., programs are published as below:

	IV semester MCA	IV semester M.Tech.	IV Semester M.Arch.	IV Semester M.Plan.	VI semester B.E./ B.Tech.
Commencement of the Semester	22.04.2024	22.04.2024	22.04.2024	22.04.2024	29.04.2024
Commencement of Classes	22.04.2024	22.04.2024	22.04.2024	22.04.2024	29.04.2024
Last Working day of the Semester	27.07.2024	27.07.2024	27.07.2024	27.07.2024	31.07.2024
Practical / Viva-Examination/Internship Viva Voce	28.07.2024 To 29.07.2024				01.08.2024 To 10.08.2024
Theory Examinations	01.08.2024 To 23.08.2024	01.08.2024 To 23.08.2024	29.07.2024 To 02.08.2024	01.08.2024 To 23.08.2024	12.08.2024 To 14.09.2024
Project viva	Will be announced after the submission of the Thesis				---
Submission of the report to university	13.07.2024 To 27.07.2024	01.08.2024 To 20.08.2024	01.08.2024 To 10.08.2024	01.08.2024 To 10.08.2024	----
Commencement of NEXT Semester	---	---	---	---	## 23.09.2024

Commencement of the swapped VII/VIII semester. 50% strength of the students may take up an Internship (VIII sem) immediately after 14.09.2024 and the remaining 50% strength of the students may take up VII semester (23.09.2024)

The principals of all the colleges are hereby informed to bring the content of the NOTIFICATION to the notice of all concerned.

Sd/-
REGISTRAR

Please Note:

- If required, the college can plan to have extra classes on 1st and 3rd Saturdays and Sundays to complete academic activities within the academic duration mentioned.
- Notification regarding the Calendar of Events relating to the conduct of University **Examinations** will be issued by the Registrar (Evaluation) from time to time.
- Academic Calendar **may be modified** based on guidelines/directions issued in the future by UGC/AICTE/State Government.
- The faculty/staff shall be available to undertake any work assigned by the university.
- If any suggestions/clarification please email–**registrar@vtu.ac.in**

To,

The Principals of all the Engineering Collegesunder the ambit of the university
The Chairpersons/Program coordinators of the University Departments at Kalaburgi, Bengaluru, Mysuru and Belagavi

Copy to.

1. To the Hon'ble Vice-Chancellor through the secretary to VC, VTU Belagavi for information
2. The Registrar (Evaluation), VTU Belagavi for information and needful.
3. The Regional Directors (I/c) of all the regional offices of VTU for circulation.
4. The Director ITI SMU, VTU Belagavi for information and to make arrangements to upload the Academic Calendar on the VTU web portal.
5. The Director of Physical Education, VTU Belagavi for information
6. The Director, Central Placement Cell, VTU Belagavi for information
7. The Special Officer Library, VTU Belagavi for information
8. All the concerned Special Officer/s and Caseworker/s of the academic section, VTU, Belagavi.
9. Office copy

15/04/24

REGISTRAR

Tentative Revised-Academic Calendar for III and IV Semesters of B.E./B.Tech., programs for the year 2023-24

	Regular Admitted Students	Lateral Entry (Diploma Graduate) Students	Working Professional (Diploma Graduates)	Remarks (Only applicable for Students admitted under working professional Category)
Commencement of the 3rd Semester	15.11.2023		12.02.2024	
Commencement of Classes	15.11.2023		12.02.2024	
Last Working day of the 3rd Semester	09.03.2024		13.04.2024	Students have to complete Theory CIE only and Practical CIE and SEE examination.
Practical Examination (Regular Students)	30.03.2024 To 12.04.2024			
Theory Examinations	13.03.2024 To 27.03.2024			
Commencement of 4th Semester	15.04.2024		15.04.2024	
Commencement of the 4th Semester and class	15.04.2024			Students have to complete Theory SEE within 15 days at the beginning of the 4th semester
Last Working day of the Semester	27.07.2024			
Practical Examination (Regular Students)	29.07.2024 to 07.08.2024			Common to all
Theory Examinations	08.08.2024 to 28.08.2024			Common to all
Practical Examinations (For Lateral Entry Students)	-----			
Commencement of 5th Semester	02.09.2024			

Please Note:

- If required, the college can plan to have extra classes on 1st and 3rd Saturdays and Sundays to complete academic activities within the academic duration mentioned. For regular and lateral entry, students' academic activities should be conducted as per the academic calendar mentioned above.

	M.S. Engineering College Bangalore Title: Calendar of Events-Even-IV SEM (April 2024 – July 2024)	Form No.: R/ PP-02/ 12/ 01

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

WEEK NO.	MONTH	DAYS						TOTAL NO. OF WORKING DAYS		EVENTS
		MON	TUE	WED	THU	FRI	SAT	General	Cumulative	
1	April 2024	22 CoS	23	24	25	26 GH	27	5	5	26th Election
2		28	29	30				3	8	
3	May 2023			1 GH	2	3	4	2	10	1st Labour Day
4		6	7	8	9	10 GH	11 MA	6	16	10th Basava Jayanthi
5		13	14	15	16	17	18	5	21	29th, 30th & 31st IA1 Test
6		20	21	22	23	24	25 MRS	6	27	
7		27 QPS, MAR, TD	28	29 IA1	30 IA1	31 IA1, CTM		5	32	
8	June 2024						1	0	32	27th, 28th & 29th IA2 Test
9		3 SF	4	5	6	7	8 MA	6	38	
10		10	11	12	13	14	15	5	43	
11		17	18	19	20	21	22 MRS	6	49	
12		24 QPS, MAR, TD	25	26	27 IA2	28 IA2	29 IA2, CTM	6	54	

REGISTRAR

	July 2024	1 SF	2	3	4	5	6	5	59	16th Muharram
14		8	9	10	11	12	13 MRS	6	65	23rd, 24th & 25th IA3 Test
15		15	16 GH	17	18	19	20	5	72	
16		22 QPS, MAR, TD	23 IA3	24 IA3	25 IA3	26 SF, CTM	27 LWD, IMS	6	78	
17		29 FIMS	30 BBS	31						
	Total Working Days								78	

Course: BE

CoS : Commencement of Semester	IA: Internal Assessment	GH: Government Holiday	MA – mentoring Activity
IMS : Internal Marks Submission	QPS : Question Paper Submission	DM : Department Meeting	BBS: blue Book Submission
MRS: Mentor Report Submission	EL: Expert lecture	FIMS: Final Internal Marks Submission	LWD: Last Working Day
SO: Saturday Off	CTM: Class Teacher Meeting	MAR : Monthly Attendance Report	SF : Students Feedback

Prepared by: Mrs. Harshitha S.P.
Designation: Assistant Professor

Signature

Approved by: Dr. Mahesh S.H
Designation: HOD

Signature

	M.S. Engineering College Bangalore Title: Calendar of Events-Even-VI SEM (April 2024 – July 2024)	Form No.: R/ PP-02/ 12/ 01

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

WEEK NO.	MONTH	DAYS						TOTAL NO. OF WORKING DAYS		EVENTS
		MON	TUE	WED	THU	FRI	SAT	General	Cumulative	
1	April 2024		29 COS	30				2	2	
3				1 GH	2	3	4	2	10	1st Labour Day
4		6	7	8	9	10 GH	11 MA	6	16	10th Basava Jayanthi
5	May 2023	13	14	15	16	17	18	5	21	
6		20	21	22	23	24	25 MRS	6	27	
7		27	28	29	30	31 CTM		5	32	
8							1	0	32	6th, 7th & 8th IA1 Test
9		3	4 QPS, MAR, TD	5	6 IA1	7 IA1	8 IA1, MA	6	38	
10	June 2024	10 SF	11	12	13	14	15	5	43	
11		17	18	19	20	21	22 MRS	6	49	
12		24	25	26	27	28	29 CTM	6	54	
13	July 2024	1 QPS, MAR, TD	2	3 IA2	4 IA2	5 IA2	6	5	59	16th Muharram

14		8 SF	9	10	11	12	13 MA	6	65	3rd, 4th & 5th IA2 Test
15		15	16 GH	17	18	19	20	5	72	
16		22	23 QPS, MAR, TD	24	25	26 IA3	27 IA3, MRS	6	78	
17		29 IA3	30 SF, IMS, CTM	31 LWD, FIMS, BBS				3	81	
	Total Working Days								81	

Course: BE

CoS: Commencement of Semester	IA: Internal Assessment	GH: Government Holiday	MA – mentoring Activity
IMS: Internal Marks Submission	QPS: Question Paper Submission	DM: Department Meeting	BBS: blue Book Submission
MRS: Mentor Report Submission	EL: Expert lecture	FIMS: Final Internal Marks Submission	LWD: Last Working Day
SO: Saturday Off	CTM: Class Teacher Meeting	MAR: Monthly Attendance Report	SF: Students Feedback

Prepared by: Mrs. Harshitha S.P.
Designation: Assistant Professor

Signature

Approved by: Dr. Malatesh S.H
Designation: HOD

Signature

	M.S. Engineering College Bangalore Title: Calendar of Events-Odd -III SEM (Nov 2023 – March 2024)	Form No.: R/ PP-02/ 12/ 01

REGISTRAR

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING / AIML

WEEK NO.	MONTH	DAYS						TOTAL NO. OF WORKING DAYS		EVENTS
		MON	TUE	WED	THU	FRI	SAT	General	Cumulative	
1	November 2023	13 COS	14	15	16	17	18	4	4	
2		20	21	22	23	24	25	6	10	12th & 13th Diwali
3		27	28	29	30 GH			4	14	30th Kanakadas Jayanthi
4	December 2023					1	2	1	15	21st CSE Club Activities
5		4	5	6	7	8	9	6	21	25th Christmas
6		11	12	13	14	15	16	5	26	
7		18	19	20	21	22	23	6	32	
8		25 GH	26	27	28	29	30	5	37	
9	January 2024	1	2	3	4	5	6	5	42	15th Makara Sankaranti
10		8	9 QPS	10	11 IA1	12 IA1	13	6	48	26th Republic Day
11		15 GH	16	17	18	19	20	4	52	IA1 Test
12		22	23	24	25	26 GH	27	5	57	

13		29	30	31				3	60	
14					1	2	3	2	62	5th Expert Talkative on MSME Schemes
15		5	6	7	8	9	10	6	68	
16	February 2024	12	13	14 IA2	15 IA2	16	17	5	73	IA2 Test
17		19	20	21	22	23	24	6	79	
18		25	26	27	28	29				
19						1	2			IA3 Test
20		4 IA3	5 IA3	6	7	8	9 LWD			
	Total Working Days								83	

Course: BE

CoS : Commencement of Semester	IA: Internal Assessment	GH: Government Holiday	MA – mentoring Activity
IMS : Internal Marks Submission	QPS : Question Paper Submission	DM : Department Meeting	BBS: blue Book Submission
MRS: Mentor Report Submission	EL: Expert lecture	FIMS: Final Internal Marks Submission	LWD: Last Working Day
SO: Saturday Off	CTM: Class Teacher Meeting	MAR : Monthly Attendance Report	SF : Students Feedback

Prepared by: Mrs. Harshitha S.P.
Designation: Assistant Professor

Signature

Approved by: Dr. Malatesh S.H
Designation: HOD

Signature

REGISTRAR

	M.S. Engineering College Bangalore Title: Calendar of Events-Odd -V SEM (Nov 2023 – March 2024)	Form No.: R/ PP-02/ 12/ 01

REGISTRAR

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING / AIML

WEEK NO.	MONTH	DAYS						TOTAL NO. OF WORKING DAYS		EVENTS
		MON	TUE	WED	THU	FRI	SAT	General	Cumulative	
1	November 2023	13 COS	14	15	16	17	18	4	4	
2		20	21	22	23	24	25	6	10	12th & 13th Diwali
3		27	28	29	30 GH			4	14	30th Kanakadas Jayanthi
4	December 2023					1	2	1	15	21st CSE Club Activities
5		4	5	6	7	8	9	6	21	25th Christmas
6		11	12	13	14	15	16	5	26	
7		18	19	20	21	22	23	6	32	
8		25 GH	26	27	28	29	30	5	37	
9	January 2024	1	2	3	4	5	6	5	42	15th Makara Sankaranti
10		8	9	10	11	12 QPS	13	6	48	26th Republic Day
11		15 GH	16	17 IA1	18 IA1	19 IA1	20	4	52	IA1 Test
12		22	23	24	25	26 GH	27	5	57	

		29	30	31				3	60	
14					1	2	3	2	62	5th Expert Talkative on MSME Schemes
15		5	6	7	8	9	10	6	68	IA2 Test
16	February 2024	12 QPS	13	14 IA2	15 IA2	16 IA2	17	5	73	
17		19	20	21	22	23	24	6	79	
18		26	27	28	29			4	83	
19						1	2	1	84	8th Maha Shivaratri
20	March 2024	4	5	6	7 QPS	8 GH	9	5	89	IA3 Test
		11 IA3	12 IA3	13 IA3	14	15	16 LWD	5	94	
	Total Working Days								94	

Course: BE

CoS : Commencement of Semester	IA: Internal Assessment	GH: Government Holiday	MA – mentoring Activity
IMS : Internal Marks Submission	QPS : Question Paper Submission	DM : Department Meeting	BBS: blue Book Submission
MRS: Mentor Report Submission	EL: Expert lecture	FIMS: Final Internal Marks Submission	LWD: Last Working Day
SO: Saturday Off	CTM: Class Teacher Meeting	MAR : Monthly Attendance Report	SF : Students Feedback

Prepared by: Mrs. Harshitha S.P.
Designation: Assistant Professor

Signature

Approved by: Dr. Malatesh .S .H
Designation: HOD

Signature

MS Engineering College, Bangalore

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

Course Information File

Semester & Year: III & 2023

Subject Name: **Digital Design and Computer Organization**	*Subject Code*: BCS302
Total Teaching Hours: **40 hrs.**	*Duration of Exam*: 03
Exam Marks: **50**	*IA Marks*: **50**
Lesson Plan Author: **Mrs. Sneha Jewargi**	
Designation: **Assistant Professor**	
Number of times taught this subject :1	
Verified by:	*Date*: 06/03/2023

Course objectives:

- To demonstrate the functionalities of binary logic system
- To explain the working of combinational and sequential logic system
- To realize the basic structure of computer system
- To illustrate the working of I/O operations and processing unit

Course Outcomes: At the end of the course, the student will be able to:

Sl. No	Course Outcomes	Bloom's Taxonomy Level
CO1	Apply the K–Map techniques to simplify various Boolean expressions.	L1
CO2	Design different types of combinational and sequential circuits along with Verilog programs.	L2
CO3	Describe the fundamentals of machine instructions, addressing modes and Processor performance.	L3
CO4	Explain the approaches involved in achieving communication between processor and I/O devices.	L4
CO5	Analyze internal Organization of Memory and Impact of cache/Pipelining on Processor Performance.	L5

Teaching Pedagogy:

1. Lecture.
2. Assignment.
3. Class Discussion.
4. Course Examination.
5. Tutorial.
6. Quiz.
7. Seminars

Mapping of Graduate Attributes to Course Outcomes (COs):

	Program Outcomes												Program Specific Outcomes	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
Course Outcomes	Engineering knowledge	Problem analysis	Design/development of solutions	Conduct investigations of complex problems	Modern tool usage:	The engineer and society:	Environment and sustainability	Ethics	Individual and team work	Communication	Project management and finance:	Life-long learning	solving Skill Problem	Professional Skill
CO1:	L	M	M										M	
CO2:	M	M	M	M							L	L	M	M
CO3:	M	L	M	L							L	M	M	L
CO4:	M	M	M								L	M	M	M
CO5:	H	L	M	L							L	M	M	M

Degree of Compliance:

High (H) : Greater than 70%
Medium (M) : Between 40 to 69%
Low (L) : Between 00 to 39%

Syllabus Content

Subject Code: BCS302 **IA: 50**

Subject Name: Digital Design and Computer Organization **Exam Marks: 50**

Teaching Hours: 40

Topics	Hours	% of Portion Covered	
		Chapter wise	Cumulative
Module – 1 **Introduction to Digital Design:** Binary Logic, Basic Theorems And Properties Of Boolean Algebra, Boolean Functions, Digital Logic Gates, Introduction, The Map Method, Four-Variable Map, Don't-Care Conditions, NAND and NOR Implementation, Other Hardware Description Language – Verilog Model of a simple circuit	08 hours	20	20
Module – 2 **Combinational Logic:** Introduction, Combinational Circuits, Design Procedure, Binary Adder- Subtractor, Decoders, Encoders, Multiplexers. HDL Models of Combinational Circuits – Adder, Multiplexer, Encoder. **Sequential Logic:** Introduction, Sequential Circuits, Storage Elements: Latches, Flip-Flops.	08 hours	20	40
Module – 3 **Basic Structure of Computers:** Functional Units, Basic Operational Concepts, Bus structure, Performance – Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement. **Machine Instructions and Programs:** Memory Location and Addresses, Memory Operations, Instruction and Instruction sequencing, Addressing Modes.	08 hours	20	60
Module – 4 **Input/output Organization:** Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Direct Memory Access: Bus Arbitration, Speed, size and Cost of memory systems. Cache Memories – Mapping Functions.	08 hours	20	80
Module – 5 **Basic Processing Unit:** Some Fundamental Concepts: Register Transfers, Performing ALU operations, fetching a word from Memory, Storing a word in memory. Execution of a Complete Instruction.	08 hours	20	100

Pipelining: Basic concepts, Role of Cache memory, Pipeline Performance.			

TEXT BOOKS:

1. M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.
2. Carl Hamacher, ZvonkoVranesic, SafwatZaky, Computer Organization, 5 th Edition, Tata McGraw Hill.

Web links and Video Lectures (e-Resources):
https://cse11-iiith.vlabs.ac.in/

EVALUATION SCHEME:

IA SCHEME	
Assessment	**Weightages in Marks**
Internal Assessment Exam 1	25
Internal Assessment Exam 2	25
Improvement- Internal Assessment Exam 3	25
Final Internal Assessment Marks	Average of Two
Assignments/Seminar etc	10
Total (Average + Assignment/Seminar etc)	25
Laboratory Record & conduction of experiment	15
Lab test	10
Total	25
IPCC Total	50

SUBJECT UTILIZATION FOR IA EXAMS:

Module	Chapter	Teaching Hours	No. of Questions in		
			IA Exam I	IA Exam II	IA Exam III
1, 2	Introduction to Digital Design	10	VTU Exam Pattern (Answer any two full questions choosing any one question from each part)		
	Combinational logic and sequential logic	10			
3, 4	Basic structure of computers and Instructions and programs	10			
	Input/Output Organization	10			
5	Basic Processing unit Pipelining	10			

Module Wise Plan

Subject Name: Digital Design and Computer Organization **Subject Code: BCS302**

Module Name and Title: 1. Introduction to Digital design

Learning Objectives:

At the end of this chapter student should be able to:

1. Explain the basic theorem and properties of Boolean algebra.
2. Design the digital logic gates.
3. Perform the k-map problems.
4. Explain the NAND and NOR gate implementation.
5. Explain the steps in HDL program.

Learning Outcomes:

1. Understanding the digital logic gates
2. Understanding how to solve K-map using different variables.
3. Understanding how to implement NAND and NOR gates.
4. Understanding the steps of HDL programming.

Lesson Schedule:

Class Number	Portion covered	Book	Page No.
1	Introduction to Digital Design: Binary Logic, Basic Theorems And Properties Of Boolean Algebra.	T1	30-50
2	Boolean Functions, Digital Logic Gates.	T1	45-65
3,4	Introduction, The Map Method, Three-Variable K-map	T1	73-79
5,6	Four variable K-map.	T1	80-87
7,8	Don't care conditions.	T1	88-90
9	NAND and NOR Implementation.	T1	90-102
10	Other Hardware Description Language – Verilog Model of a simple circuit.	T1	108-118

	Questions	Blooms Taxonomy
1	With symbol, truth table and Boolean expression explain a) AND gate b) OR gate c) NOT gate d)XOR gate e)NAND GATE	L1
2	Explain basic theorem and properties of Boolean algebra?	L1
3	Realize the function using only two input NAND gate and inverter i) $f1=\sum m(0,2,3,4,5)$ ii) $f2=\sum m(1,2,6,7)$	L1
4	$F(P, Q,R,S)=\sum m(0,3,5,6,7,11,14)$. Write the SOP and logic diagram.	L2
5	$F(A,B,C,D)=\sum m(1,2,3,5,6,7,11,12,13,14,15)$. Draw the logic diagram.	L2
6	$F(w,x,y,z)=\sum m(7,9,12,13,14,15)+d(4,11)$	L2
7	$F(ABCD)=\sum m(0,1,2,3,10,11,12,13,14,15)$	L2
8	Realize the given function $F=\overline{bc}+a\overline{b}+\overline{a}b$	L2

9 $F(WXYZ)=\overline{XZ}+WYZ+\overline{WYZ}+\overline{XY}$. Realize the given function L2

10 $Y = ABCD+ \overline{ABCD} + A\overline{BC} + \overline{AB}$ L2

Module Name and Title: 2. Combinational and Sequential circuit

Learning Objectives:

At the end of this chapter student should be able to:

1. Explain the combinational circuit.
2. Explain how to design Adder and Subtractor.
3. Explain the decoder, encoder and multiplexer.
4. Explain the steps to write HDL program code.
5. Explain the Methods of sequential circuit.
6. Explain the implementation of latches and flip-flops.

Learning Outcomes:

1. Understanding the combinational circuit.
2. Understanding how to implement Adder, Subtractor.
3. Understanding how to design Decoder, Encoder and Multiplexer.
4. Understanding the steps to write HDL programs.
5. Understanding the design method of sequential circuit.
6. Understanding the design concept and implementation of latches and flip-flops.

Lesson Schedule:

Class Number	Portion covered	Book	Page No.
11	**Introduction: Combinational Circuits**	T1	125-127
12	Design Procedure: Binary Adder	T1	129-141
13	Subtractor, Decoders	T1	141-154
14	Encoders, Multiplexers	T1	155-163
15	HDL Models of Combinational Circuits – Adder, Multiplexer, Encoder.	T1	164-181
16	Sequential Logic: Introduction, Sequential Circuits.	T1	190-192
17	Storage Elements: Latches	T1	193-196
18	Flip-Flops.	T1	196-203

	Questions	Blooms Taxonomy
1	Design a Full adder by constructing truth table, logic diagram and simplify the output equation.	L2
2	Design and explain half substractor.	L2
3	Explain the working principle of 4 bit binary adder with carry propagation.	L2
4	Explain multiplexer with the help of logic diagram and corresponding expression.	L2
5	Briefly explain with neat diagram 3:8 decoder.	L2
6	Explain in brief history of HDL and structure of HDL module.	L1
7	Explain the full substractor with circuit diagram and expression.	L2
8	What is VHDL? show how to model 4:1 MUX using VHDL conditional assignment statement.	L2
9	Using structural model, write VHDL code for Half adder	L2
10	Explain structure of VHDL program. Write VHDL code for 4-bit parallel adder using full adder as component.	L2
11	Explain working of SR latch using NOR gates.	L3
12	Explain with neat diagram, working of JK flip flop and derive the characteristics equation.	L3
13	Derive characteristics equation for the following flip flops i) SR flip flop ii) D flip flop iii) T flip flop iv) JK flip flop	L3

Module Name and Title: 3. Basic structure of computers

Learning Objectives:

At the end of this chapter student should be able to:

1. Explain the meaning and types of functional units of computer.
2. Explain the Stages of bus structure.
3. Explain the Role of performance of clock in processor.
4. Explain the machine instructions and program.
5. Explain different types of addressing modes.

Learning Outcomes:

1. Understanding the meaning and operational concepts.

2. Understanding the Performance of processor clock.
3. Understanding the machine instruction and program.
4. Understanding the instruction and addressing modes.

Lesson Schedule:

Class Number	Portion covered	Book	Page No.
19	Functional Units, Basic Operational Concepts.	T2	2-7
20	Bus structure, Performance – Processor Clock	T2	9-14
21	Basic Performance Equation, Clock Rate.	T2	14-16
22	Performance Measurement, Machine Instructions and Programs.	T2	17-20
23	Memory Location and Addresses.	T2	33-36
24	Memory Operations, Instruction and Instruction sequencing.	T2	36-44
25	Addressing Modes.	T2	48-56

	Questions	Blooms Taxonomy
1	With a neat diagram describe the functional unit of computer.	L1, L2
2	Explain the basic operational concept between processor and memory with neat diagram.	L2
3	Explain various parameters that affects the performance of a computer and also provide the basic performance equation.	L2
4	Explain bus structure.	L2
5	Write a note on processor clock.	L2
6	Explain how to measure the performance of computer.	L2
7	Explain the i) one address instruction ii)two address instruction iii)three address instruction with example?	L2
8	Define byte addressability, Big-Endian and Little-Endian assignment briefly.	L2
9	Explain memory location addressing.	L2
10	Explain memory operation with example.	L2
11	Illustrate instruction and instruction sequential with example.	L2
12	Explain conditional codes with example.	L2
13	Discuss the following addressing modes with example i) Immediate ii) Register iii)Direct iv)Indirect v)Index	L2

Module Name and Title: 4. Input/output Organization

Learning Objectives:

At the end of this chapter student should be able to:

1. Explain the memory mapping and I/O mapping.
2. Explain the need of Interrupt.
3. Explain the Direct Memory Access.
4. Explain the concept of Bus Arbitration.
5. Explain the cache memory and memory mapping.

Learning Outcomes:

1. Understanding the memory mapping and I/O mapping.
2. Understanding the significance of Interrupt.
3. Understanding the concept of Direct memory Access.
4. Understanding the importance of Bus Arbitration.
5. Understanding the concept of cache memory and memory mapping.

Lesson Schedule:

Class Number	Portion covered	Book	Page No.
26	Accessing I/O Devices	T2	204-205
27	Interrupts – Interrupt Hardware	T2	205-210
28,29	Enabling and Disabling Interrupts, Handling Multiple Devices.	T2	211-213
30	Direct Memory Access	T2	234-236
31	Bus Arbitration	T2	237-240
32	Speed, size and Cost of memory systems.	T2	313
33	Cache Memories	T2	313-315
34	Mapping Functions	T2	316-321

	Questions	Blooms Taxonomy
1	Write a note on single bus structure with neat diagram.	L2
2	Explain the concept of memory map I/O and I/O interface with neat diagram.	L1

3	Write a note on i) Interrupt hardware ii) Interrupt nesting.	L2
4	Explain the following i)vector interrupt ii) simultaneous request .	L2
5	Define interrupt. Point out and explain the various types of enabling and disabling interrupt.	L2
6	Explain the following method of handling interrupt from multiple devices. (i) Diasy chain (ii) Priority structure.	L2
7	Explain operation of DMA with neat diagram.	L2
8	Define Bus arbitration? Explain centralized arbitration mechanism in DMA with a neat diagram.	L2
9	Explain the distributed arbitration mechanism in DMA with a neat diagram.	L2
10	Define cache memory? Explain various types with neat diagram.	L2
11	What is mapping? Explain set associative technique with neat diagram.	L2
12	What is cache memory? Explain direct mapping.	L2

Module Name and Title: 5. Basic Processing Unit

Learning Objectives:

At the end of this chapter student should be able to answer:

1. Explain the fundamental concept of processing unit.
2. Explain the steps in performing ALU operation.
3. Explain how to fetch and store a word in memory.
4. Explain the basic concept of pipelining.
5. Explain the role of cache memory.
6. Explain the pipeline performance.

Learning Outcomes:

1. Understanding the fundamental concepts of processing unit.
2. Understanding the steps in performing ALU operation and register transfer.
3. Understanding how to fetch, store and execution of a word in memory.
4. Understanding the basic concept of pipelining
5. Understanding the role of cache memory
6. Understanding the pipelining performance.