Curriculum Vitae

Dr. Cyril Prasanna Raj P. – **Dean (R&D) MS Engineering College, Bangalore**
cyrilyahoo@gmail.com/cyril@msec.ac.in

Experience:

Total years of experience: 16 Years of research/teaching experience in:

- System level design and modelling of signal and image processing applications
- VLSI design and SOC design
- Sensors and instrumentation focussing on nanoelectronic circuits and sensors for chemical and biological applications

Current Employment (August 2012-till date):

- **Dean(R&D) and Professor** – M. S. Engineering College, Bangalore
  - In charge for R&D activities at MSEC, involved in industry collaborations, research collaborations and career development training
- **Additional Responsibilities:**
  - **Director - Innovation and Entrepreneurship Development Cell, Sponsored by DST**
    - Responsible for setting up innovation cell and promoting entrepreneurship activities among students
  - **Project Coordinator, MS-TRAC:** Responsible for developing curriculum that are industry relevant and imparting industry specific training for students and assist them in placements
  - **Chief Coordinator –** Mission VTU Empower 10K (VLSI Design and Embedded Systems)
    - Formulation of industry relevant course, selection of students, delivery of course and placement of students

Previous Employment:

- **HOD**-Dept. of Electronics and Electrical Engineering, **MS Ramaiah School of Advanced Studies**, Bangalore **(March 2001- August 2012)**
  - Established VLSI design centre and established EEE dept. at MSRSAS
  - Involved in R&D activities and Administrative activities
- **Lecturer**, GVIT, KGF **(July 1999-February 2001)**

Entrepreneur:

1. **Sanaris Technologies**, working as **Director** of the company which was started in the year 2008
   - **Responsibility:** Mentoring team of 6 engineers is involved in developing FPGA IPs in the areas of signal processing, image processing and communications. Driving another 5 member team in product development and commercialization.
2. **Nazrene Power Systems, Bangalore** started in the year 1996 and was involved in design and deployment of emergency home lighting units. The emergency light was indigenously designed and tested using available circuits and more than 500 units were sold in Kolar.
3. **MS Energen Pvt. Ltd – Director (Technical), Electronic Product Development**

Funded Research Projects/Grants:

1.ISRO Project (Completed) (2007):

a. **Principal investigator:** High speed architectures for Image Compression and Decompression on Reconfigurable Platforms for Launch Vehicle Applications

b. **Funding organization:** VSSC, Trivandrum
c. **Project Scheme:** Respond Project (Three Years)

2. **DST-NSTEDB-IEDC (45 Lakhs)**: Five Years Grant from DST for five innovative projects.
3. **AICTE RPS Scheme (27 Lakhs)(2013-2015)**
   a. **Principal Investigator:** Bioinspired autonomous navigation**(In Progress)**
4. **VGST-CSESM (60 lakhs)** (**2013-2015**)
   a. Principal Investigator (Underwater Navigation Sensors)
5. **DRDO Research Project on Brain Computer Interface (In Progress)**
6. TRIP-VGST Grant: Online pollution monitoring for navigation assistance(**Completed:2013**)
7. **AICTE FDP Grant**: Program coordinator for FDP on Research Methodology (**Completed:2013**)
8. **DST FDP Grant:** Program Chair for FDP on Advances in Nano and Micro Systems (**Completed:2013**)
9. VGST-VTU grant for FDP on VLSI SOC Design (**Completed:2013**)

Memberships:

- **ISTE: Member**
- **IEEE: Senior Member**
- **Member, BOE**: (ECE/TC) VTU, Belgaum
- **Member**, **BOS**: (ECE) Reva University
- **Member, BOS:** SVCET, Chittoor, AP
- **Adjunct Faculty**: ESCI, Hyderabad

Awards/significant achievements:

- Receiver of UKERI Funding for two successive years and visited Coventry University, Warwick University, Oxford University, Cambridge University, UK
- Developed India's first VLSI design software (Copyright with MSEC)
- Developed India's first nanoelectronic circuit design software (Copyright with MSEC)
- Developed Interactive E-Learning software for first year engineering
- Received Xilinx/Cypress university grants worth 1.5 crore for setting up of Xilinx and PSOC lab
- Best project award in Cypress Design Contest
- Incubated seven companies in the field of product design, software services
- Established Indias first real time virtual lab in the field of VLSI and embedded systems design

PhD Supervision:

- Registered Guide under VTU, Belgaum with 3 students registered in 2013, and 3 students in 2014 currently pursuing PhD, 3 students in 2015

M.Tech:

- Supervised more than 300 students in M. Tech Project work

Education/Qualification:

- PhD from Coventry University, UK in VLSI Signal Processing (2011)
- M.Tech in Industrial Electronics from KREC, Surathkal, Karnataka (1999)
- B.E in ECE from SJCE Mysore (1996)

Corporate Trainer For:

Tejas Networks, Honeywell, Intel, Sasken, Robert Bosch, Synopsys, Tata Motors, Tech Mahindra, Tektronix, Purple Vision, Mindtree, Tata Elxsi, LRDE, SHAR, ADE, ISRO, BEL, BEML, Mahindra etc.,

Publications and Patents: (12 Patents and more than 50 publications)

Patents:

1. Cyril Prasanna Raj et al., "BIO-INSPIRED VELOCITY ESTIMATION AND MOTION DETECTION METHOD WITH MICRO-CORE PROCESSING ENGINES FOR AUTONOMOUS NAVIGATION SYSTEM", Indian Patent Application: **1237/CHE/2015, 2015**
2. Cyril Prasanna Raj et al., "FIBRE ACOUSTO-OPTIC SENSING MANDREL WITH HIGHER PRESSURE AND SENSITIVITY", Indian Patent Application: **1238/CHE/2015, 2015**
3. Cyril Prasanna Raj et al., "SYSTEM GROUNDWATER LEVEL AND POLLUTION MONITORING WITH WIRELESS SENSOR NETWORKS INTEGRATED WITH POWER LINE COMMUNICATION", Indian Patent Application: **1959/CHE/2015, 2015**
4. Cyril Prasanna Raj et al., "REAL-TIME GPS TRACKING AND MANAGEMENT SYSTEM FOR COLLEGE TRANSPORT", Indian Patent Application: **1961/CHE/2015, 2015**
5. Cyril Prasanna Raj et al., "METHOD FOR IMPLEMENTING AN INTEGRATED DEVELOPMENT ENVIRONMENT (IDE) FOR DESIGN, MODELING AND ANALYSIS OF VLSI CIRCUITS ", Indian Patent Application: **1957/CHE/2015, 2015**
6. Cyril Prasanna Raj et al., "INTERACTIVE E-LEARNING SOFTWARE", Indian Patent Application: **1962/CHE/2015, 2015**
7. Cyril Prasanna Raj et al., "Configurable SC-FDMA Uplink Module", Indian Patent Application: 4146/CHE/2012, October 9, 2012.
8. Cyril Prasanna Raj et al., "Automotive Wing Mirror for a Car", Indian Patent Application: 3706/CHE/2012, 7th September, 2012
9. Cyril Prasanna Raj et. al, "*Wavelet Transformation Using Multicore Processors*"' Indian Patent Application: 3635/CHE/2010, November 30, 2010 International Patent Application PCT/IB2011/050167, January 14, 2011
10. Cyril Prasanna Raj et al., "*An apparatus for computation of wavelet transform using systolic arrays with low gate count, low memory, low I/O count, and energy requirements*" Indian Patent Application: 3635/CHE/2010, November 30, 2010, International Patent Application PCT/IB2011/050167, January 14, 2011
11. Cyril Prasanna Raj et al., "*Data Interface Circuit*" Indian Patent Application : 2040/CHE/2010, July 16, 2010 International Patent Application PCT/IB2010/054706
12. Cyril Prasanna Raj et al., "*Optimized Multichannel switched network interface for Multicore Processor*" Indian Patent Application: 2040/CHE/2010, July 16, 2010, International Patent Application PCT/IB2010/054706

Publications (2015-2009):

1. Mangala Gowri S .G, Navya P, Cyril Prasanna Raj. P, An Efficient Performance analysis for EEG signal Denoising and classification using Multiwavelets, International Conference on Power, Circuit and Information Technologies (ICPCIT-2015), Bangalore, 27-28 April 2015.
2. Raju Hajare, C Lakshminarayana, GH Raghunandan, Cyril Prasanna Raj P, Performance

enhancement of FINFET and CNTFET at different node technologies, Microsystem Technologies, Springer Berlin Heidelberg, pp.1-6, 2015, DOI 10.1007/s00542-015-2468-9

3. *SWETHA LAKSHMI.K, DR. CYRIL PRASANNA RAJ P, AZRA JEELANI,* Implementation of Digital Beam-forming for Underwater 2-D Sonar Imaging System, International Journal of Scientific Engineering and Technology Research, Vol. 3, Issue 12, 2014, ISSN : 2319-8885
4. *USHA.K, DR. CYRIL PRASANNA RAJ P, AZARATHAMMA.S,* An FPGA Implementation of Bio-inspired Motion Detection for Autonomous Navigation System, International Journal of Scientific Engineering and Technology Research, Vol. 3, Issue 12, 2014, pp. 2669-2671, ISSN : 2319-8885
5. *MADHURENDRA KUMAR, DR.CYRIL PRASANNA RAJ P, VINOD KUMAR B. L,* A Novel Non-Expandable Visual Cryptography with Increased Capacity, International Journal of Scientific Engineering and Technology Research, Vol. 3, Issue 12, 2014, pp. 2696-2698, ISSN : 2319-8885
6. *SUMA.C, DR. CYRIL PRASANNA RAJ P, MS.AZARATHAMMA.S*, An FPGA Implementation of Bio-Inspired High Speed Vision System for Feature Extraction, International Journal of Scientific Engineering and Technology Research, Vol. 3, Issue 12, 2014, pp. 2637-2639, ISSN : 2319-8885
7. *SUDHA.B.S, VENKATESHAPPA, DR. CYRIL PRASANNA RAJ.P,* Image Fusion by DWT Architecture for MAV Applications, International Journal of Scientific Engineering and Technology Research, Vol. 3, Issue 12, 2014, pp. 2725-2728, ISSN : 2319-8885
8. Nivedita S Khanapur, Dr. Cyril Prasanna Raj P, Mr. Vinod Kumar . B. L, Design and Implementation of an Efficient Serial- Pipelined FFT Architecture for Through Wall Image Processing on FPGA, International Journal of Engineering Research & Technology, Vol. 3 - Issue 5 (May - 2014), e-ISSN: 2278-0181
9. DEEPA KINI K. , PRASHIL M. JUNGHARE. , CYRIL PRASANNA RAJ., UNDERWATER ACOUSTIC SIGNAL SENSING USING SENSING MANDREL, International Conference on Electrical Electronics and Communications-ICEEC-21st June 2014-ISBN-978-93-81693-66-03
10. Nelojit Mayenbam, Prashil M. Jungahre, Cyril Prasanna Raj, A novel Architecture for DOA estimation of signals to track target source positions, INTERNATIONAL JOURNA L FOR RES EARCH IN AP PL I ED SC IENC E AND ENGINEERING TECHNOLO GY (IJRAS ET), Vol. 2 Issue VI, June 2014 ISSN: 2321-9653
11. Prashil M. Junghare, Dr. Cyril Prasanna Raj P, Dr. T. Srinivas, Dr. Preeta Sharan, A Finite Element Analysis of Fiber Optic Acoustic Sensing Mandrel for Acoustic pressure with Increased Sensitivity, American Journal of Engineering Research, Vol.2, Issue 9, ISSN No.:2320-0847, 2013, pp:1-7
12. Cyril Prasanna Raj P. and Lourts Deepak, Performance comparison of CMOS and FINFET based SRAM for 22nm Technology, International Journal of Conceptions on Electronics and Communication Engineering, Vol.1, Issue 1, Dec 2013, ISSN:2357-2809, pp:6-10.
13. P. Cyril Prasanna Raj, Dr. S. L. Pinjare , FPGA Implementation Of Efficient Algorithm Of Image Splitting For Video Streaming Data, International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622, Vol. 2, Issue 5, September- October 2012, pp.1244-1247
14. P. Cyril Prasanna Raj, Dr. M. Z. Kurian, Manjula. *Y,* VLSI architecture and implementation for 3D neural network based image compression, International journal of advanced research in computer engineering and technology, ISSN:2278-1323, Vol.1,

No.4, 2012

15. Cyril Prasanna Raj, Mrs. Manjula.Y, Dr. M. Z. Kurian, "VLSI Architecture Design and Implementation for 3D Neural Network based Image Compression" International Conference on Current Trends in Engineering and Management(ICCTEM-2012) VVCE, Mysore to be held on 12th, 13th & 14th July 2012
16. G Mamatha, Shaik Abdul Rahim, Cyril Prasanna Raj, Feature-Level Multi-focus Image Fusion using Neural Network and Image Enhancement, GJCST (2012) Volume 12 Issue 10, pp:17-23.
17. Cyril Prasanna Raj P., Design and Implementation of Low Power 12-Bit 100-MS/S Pipelined ADC Using Open-Loop Residue Amplification, GJRE (2012) Volume 12 Issue 11, pp:15-21
18. P. Cyril Prasanna Raj, Pillem Ramesh, B.V Aravind, Dr. Fazal, Noorbasha, Design and Performance Analysis of Analog Sub circuits for Multiplying DAC used in Image Compression, International Journal of Engineering Research and Applications (IJERA), ISSN: 2248-9622, Vol. 2, Issue 3, May-Jun 2012, pp.1213-1219
19. P. Cyril Prasanna Raj; S. Ramachandran, Modified VLSI implementation of DA-DWT for image compression, Int. J. of Signal and Imaging Systems Engineering, 2012 Vol.5, No.3, pp.167 – 174
20. Cyril Prasanna Raj P, FPGA Implementation of High Speed Area Efficient Lifting Scheme Based DWT Architecture for Image Fusion, European Journal of Scientific Research, ISSN 1450-216X Vol. 89 No 1 October, 2012, pp.64-76.
21. M Nagabushanam, P Raj, S Ramachandran, Design and FPGA implementation of modified Distributive Arithmetic based DWT-IDWT processor for image compression, Communications and Signal Processing (ICCSP), 2011 International Conference on, pp.1-4, 2011
22. YN Santhosh, Namita Palacha, Cyril Prasanna Raj, Design and VLSI Implementation of interpolators/decimators for DUC/DDC, Emerging Trends in Engineering and Technology (ICETET), 2010 3rd International Conference on, pp. 755-759, 2011
23. G Harish, S Prabhu, P Cyril Prasanna Raj, Power Effective Cascaded Flash-SAR Sub ranging ADC, IJTES, Vol. 2, Issue 3, pp. 306-308, 2011
24. K Venkata Ramanaiah, Cyril Prasanna Raj, ASIC Implementation of Neural Network Based Image Compression, vol. 3, issue 4, pp. 494-498, International Journal of Computer Theory and Engineering, 2011
25. BM Sunil, Cyril Prasanna Raj, Analysis of wavelet for 3d-dwt volumetric image compression, Emerging Trends in Engineering and Technology (ICETET), 2010 3rd International Conference on, pp. 180-185, 2011
26. Cyril Prasanna Raj, GM Reddy, Design and Verification of Cache Memory Decoder for High Speed Multicore Processor, Emerging Trends in Engineering and Technology (ICETET), 2010 3rd International Conference on, pp. 770-775, 2011
27. MB Veena, Cyril Prasanna Raj, MN Shanmukha Swamy, FPGA Based Reconfigurable 200 MHz Transmitter and Receiver Front End for MIMO-OFDM, Emerging Trends in Engineering and Technology (ICETET), 2010 3rd International Conference on, pp. 819-824, 2010
28. K Venkata Ramanaiah, Cyril Prasanna Raj, K Lal Kishore, New Architecture For NN Based Image Compression For Optimized Power, Area And Speed, 13th International Conference on Biomedical Engineering, Springer Berlin Heidelberg, pp.13-17, 2009
29. M Nagabushanam, Cyril Prasanna Raj, S Ramachandran, Design and implementation of

parallel and pipelined distributive arithmetic based discrete wavelet transform IP core, Proceedings of the European Journal of Scientific Research, Vol. 35, pp. 378-392, 2009

30. S Shanthala, Cyril Prasanna Raj, SY Kulkarni, Design and VLSI Implementation of Pipelined Multiply Accumulate Unit, Emerging Trends in Engineering and Technology (ICETET), 2009 2nd International Conference on, pp.381-386, 2009
31. Pachara V Rao, C Prasanna Raj P, S Ravi, VLSI design and analysis of multipliers for low power, Intelligent Information Hiding and Multimedia Signal Processing, 2009. IIH-MSP'09. Fifth International Conference on, pp. 1354-1357, 2009
32. PV Rao, Cyril Raj Prasanna, S Ravi, Design and ASIC implementation of root raised cosine filter, European Journal of Scientific Research, Vol. 31, Issue 3, pp. 319-328, 2009
33. Cyril Prasanna Raj P., SL Pinjare, Design and analog VLSI implementation of neural network architecture for signal processing, European Journal of Scientific Research, Vo. 27, Issue 2, pp. 199-216, 2009
34. Ganapathi Hegde, PR Vaya, Cyril Prasanna Raj P., Implementation of systolic array architecture for full search block matching algorithm on FPGA, Vol. 33, issue 4, pp. 606-616, 2009
35. Cyril Prasanna Raj P. and Pinjare, S. L.; "Analog VLSI Implementation of Novel Hybrid Neural Network Multiplier"; Architecture,3rd International conference on intelligent systems and control ISCO2009) on Microsystems technology and its applications, February, KEC, Coimbatore.(2009)
36. Cyril Prasanna Raj P., & Pinjare, S. L. ; "ASIC Implementation of Nonlinear Neural Networks for Image Compression optimizing Area and Power"; 3rd International conference on intelligent systems and control (ISCO2009) on Microsystems technology and its applications, February, KEC, Coimbatore (2009).
37. Cyril Prasanna Raj P., & Pinjare, S. L. ; "Design and Implementation of Current - Mode Hybrid Digital-to-Analog Converter" ;3rd International conference on intelligent systems and control (ISCO2009) on Microsystems technology and its applications, February, KEC, Coimbatore. (2009).
38. Gopakumar, K. S., Cyril, Prasanna Raj P. and Pinjare, S. L. ; "Design and Implementation of High Speed, Low Power 10-bit DAC for Video Application";SASTECH Journal, MSRSAS 6, 71-78. (2007)
39. Cyril Prasanna Raj P. and S. L. Pinjare,; "Multilayered neural network architecture for image compression";International Conference on Computational Intelligence and Multimedia Applications 2007 (ICCIMA '07), Sivakasi, August 2007
40. Cyril Prasanna Raj P. and S. L. Pinjare, "Design and Analog VLSI Implementation of Neural Network Architecture"; International Conference on Computational Intelligence and Multimedia Applications 2007 (ICCIMA '07), Sivakasi August 2007
41. Cyril Prasanna Raj P. and S. L. Pinjare,;"ASIC implementation of modified DADDA multipliers with minimum critical path for neural network architecture based image compression";National conference on VLSI and embedded systems, SASTRA, Tanjavur, August 2006
42. Cyril Prasanna Raj P. and S. L. Pinjare; "Design, Analysis & FPGA implementation of Multilayered Neural Network architecture for compression of multi domain Images"; National conference on VLSI, Embedded and Digital image processing image processing, IEEE TTTC v and VLSI society of India, VEDAS2005, Salem, June 2005. The paper has won the best paper award.

43. Cyril Prasanna Raj P. and S. L. Pinjare; “Design and Implementation of High Speed, Low Power 10-bit DAC for Video Application”;VDAT 2007
44. Aditya Ambardar, Cyril Prasanna Raj P. and S. L. Pinjare,; “Design and Implementation of Neural Architecture in Analog VLSI”; VDAT 07
45. Aditya Ambardar, Cyril Prasanna Raj P. and S. L. Pinjare; “Design and Implementation of Parallel and Pipelinined Distributive Arithmetic Discrete Wavelet Transform IP core”; Proceedings IP/SoC-2006 Conference,(Grenoble, France - December 6-7, 2006)

Corporate Trainer:	**Domain:**
• Robert Bosch • Synopsys • Honeywell • Tejas Networks • Sasken • Tata Elxsi • Tektronix • Purple Vision Technology • ITI • BHEL • BEML • LRDE • SHAR • ISRO • Tata motors • Dexel	• FPGA • MATLAB • Automotive Electronics • Verilog/VHDL • State Models • Neural Networks • Artificial Intelligence • Image Processing • Communication Systems • Signal Processing • PID Controllers • Mixed Signal Design • Analog IC Design • Layout Design • ASIC Design • CMOS Circuits