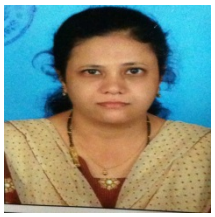
Curriculum –Vitae

<table>
<tr><td>1.</td><td>Name:
  </td><td>Azra Jeelani</td></tr>
<tr><td>2</td><td>Address and Contact Numbers</td><td>#17, Mathru Layout, 7th cross, Yelahanka New Town, Pin No:560065</td></tr>
<tr><td>3.</td><td>Date of Birth/Sex/Marital Status</td><td>07/07/1974/ Female/ Married</td></tr>
<tr><td>4.</td><td>Affiliation</td><td>Associate Professor, MSEC, Bangalore</td></tr>
<tr><td>5.</td><td>Educational Qualification</td><td>
<table>
<tr><th>Degree</th><th>year</th><th>University/College</th><th>Results</th></tr>
<tr><td>BE</td><td>1997</td><td>Gulbarga University/ SLNCE, Raichur</td><td>First Class</td></tr>
<tr><td>M.Tech</td><td>2010</td><td>VTU/ Sir.MVIT, Bangalore</td><td>First Class</td></tr>
<tr><td>Registered Ph.D</td><td></td><td>VTU</td><td></td></tr>
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<tr><td>6.</td><td>Experience</td><td>
<table>
<tr><th>College</th><th>From</th><th>To</th><th>Years</th></tr>
<tr><td>SVITS, Mbnr, AP</td><td>19/2/2001</td><td>30/09/2005</td><td>4.8Yrs</td></tr>
<tr><td>SVCE, Bangalore</td><td>1/10/2005</td><td>6/09/2008</td><td>3 Yrs</td></tr>
<tr><td>BCE, Bangalore</td><td>2/08/2010</td><td>30/11/2010</td><td>0.4 Yrs</td></tr>
<tr><td>MSEC,Bangalore</td><td>22/7/2011</td><td>Till Date</td><td>3 Yrs</td></tr>
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</td></tr>
<tr><td>7.</td><td>Subject Areas of Interest</td><td>CommunicationSystems, VLSI, Image Processing</td></tr>
<tr><td>8.</td><td>Research Projects Worked and Grants Received</td><td>Clock Period Minimization of circuit using Retiming Transform.</td></tr>
<tr><td>9.</td><td>Consultancy Projects Worked</td><td></td></tr>
<tr><td>10.</td><td>Number of Projects/Thesis Supervised
• Masters
• PhD</td><td>Implementation of cordic algorithm on Adaptive digital beamforming</td></tr>
<tr><td>11.</td><td>Publications and Patents (Details can be added in annexure)</td><td>
<table>
<tr><td>1</td><td>Conference</td><td>2</td></tr>
<tr><td rowspan="3">2</td><td>Journals</td><td>1</td></tr>
<tr><td>National</td><td>1</td></tr>
<tr><td>International</td><td>1</td></tr>
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		3	Invited Talks	
		4	Patents	
		5	Any other	
12.	Membership of Professional Bodies			
13.	Awards if Any			
14.	Any other Achievements			

Annexure :

National/International Conference

1. Underwater remotely operated vehicle for drowned body detection. (National Conference of Advanced Research in Electronics & Communication engineering-2014)
2. A review on security chip in a biometric passport using cryptography.(NCAREC-1014)
3. Development of CAD tool for Clock Period Minimization using Retiming Transform.(International Conference on Electrical, Electronics and Communication , Chirala, IIST-2014)

Workshop Conducted/ Attended

1. Three day workshop (7^{th}-9^{th}Feb 2013) on "FPGA based signal and image processing applications", at MSEC.
2. One day workshop (10 nov 2012) on "Android based application development", at MSEC.
3. Two day workshop (15^{th}-16^{th}March 2013) on "Speech processing robots using MSP430 microcontroller".
4. Workshop (Aug.2007) on "Digital system design using verilog/vhdl and FPGA", at SVCE.
5. Staff development program on "Teaching methodologies", at SVCE.
6. Faculty Development Program (24^{th}-26^{th} Aug,2010) on "Micro strip Antennas and Advanced communication", at Sir MVIT college.
7. Workshop of 6 days (14^{th}-19^{th} July 2014) on "Trends in Underwater Acoustics Communication and SONAR" at R.V College of Engineering, Bangalore.
8. FDP of 3 days(22^{nd}-24^{th} january,2014) on "Research Process, technical paper writing and Patenting", by R& D centre, MSEC.

Journal /Publication :

1. Development of CAD tool for Clock Period Minimization using Retiming Transform. (International Conference on Electrical, Electronics and Communication , Chirala, IIST)